

Hadley14'' Schematics Document

Haswell ULT

2013-08-14

REV : A00

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DY : None Installed

<Core Design>



Wistron Corporation
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Title

Cover Page

Size
A3

Document Number

Hadley 14''

Rev
A00

Date: Wednesday, August 14, 2013

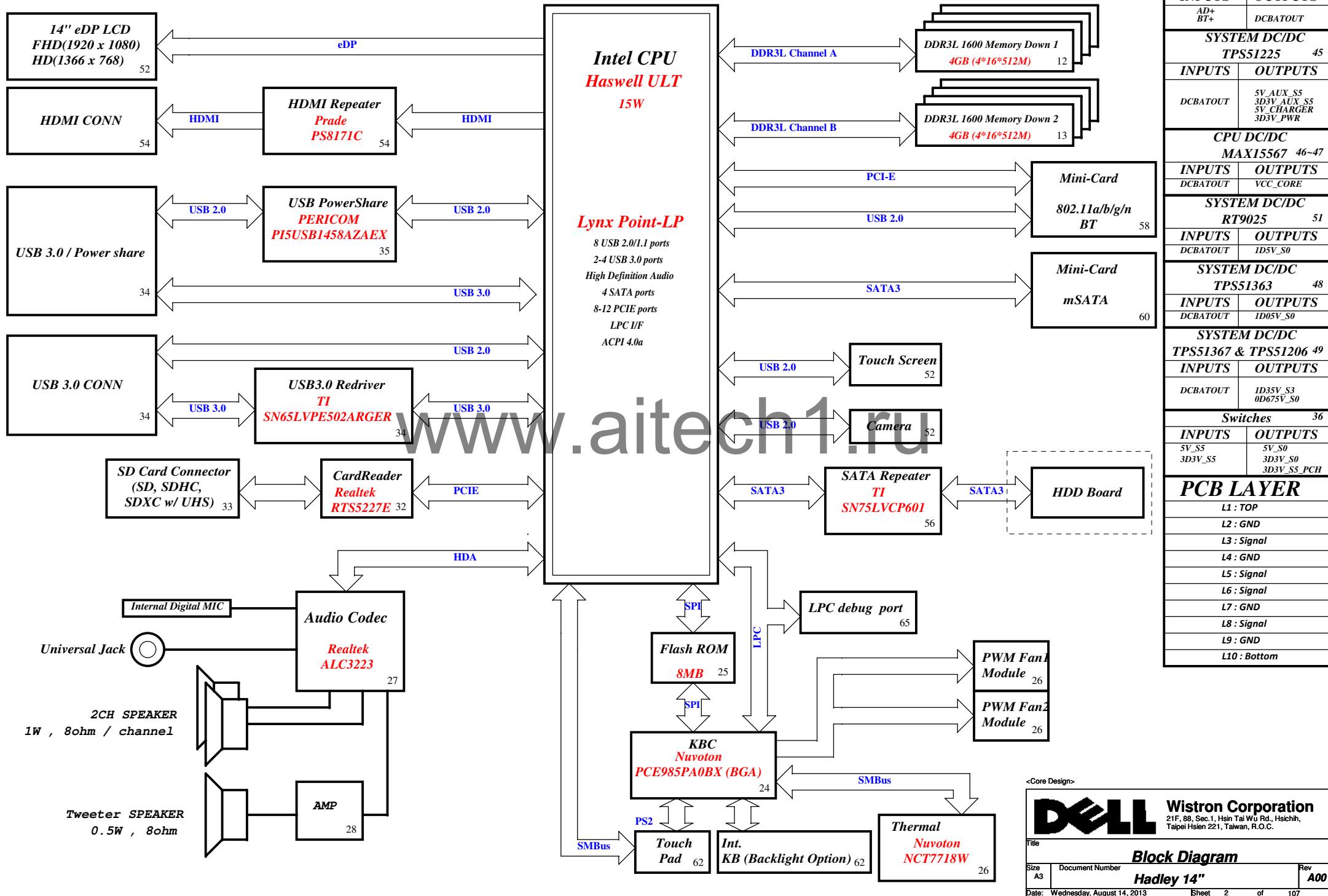
Sheet 1 of 107

Hadley 14 Block Diagram

Project code : 91.46L01.001

PCB P/N : 12310


Revision : SB



(Blanking)

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Size

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Hadley 14"

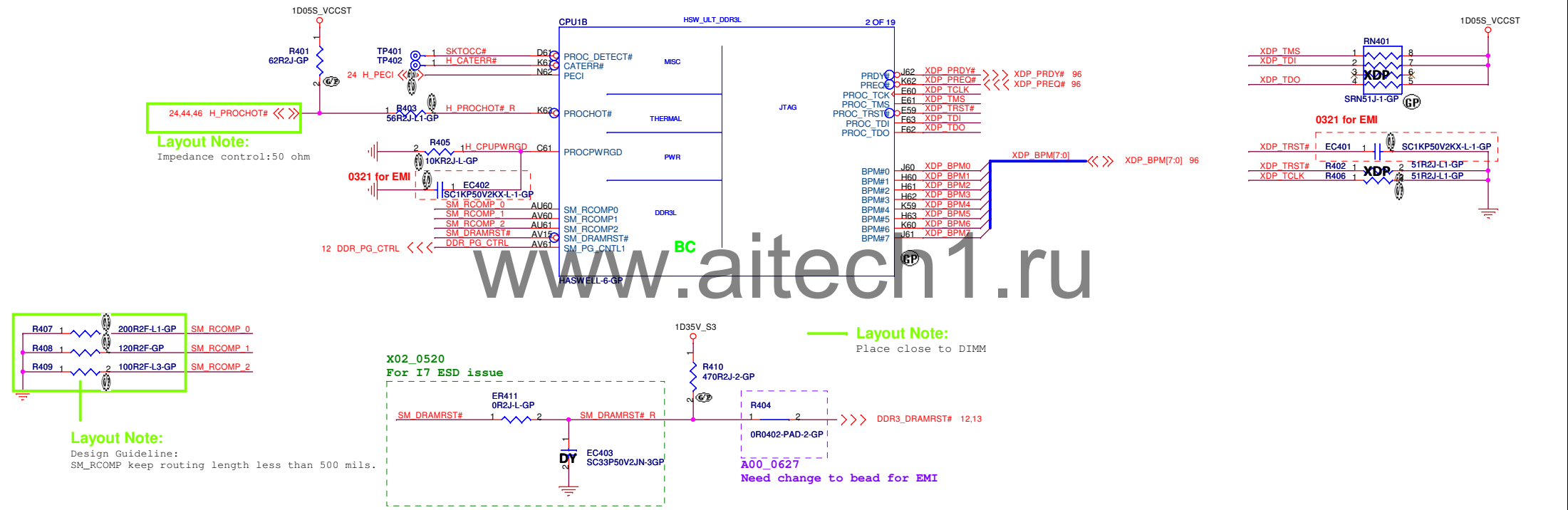
Date: Wednesday, August 14, 2013

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SSID = CPU

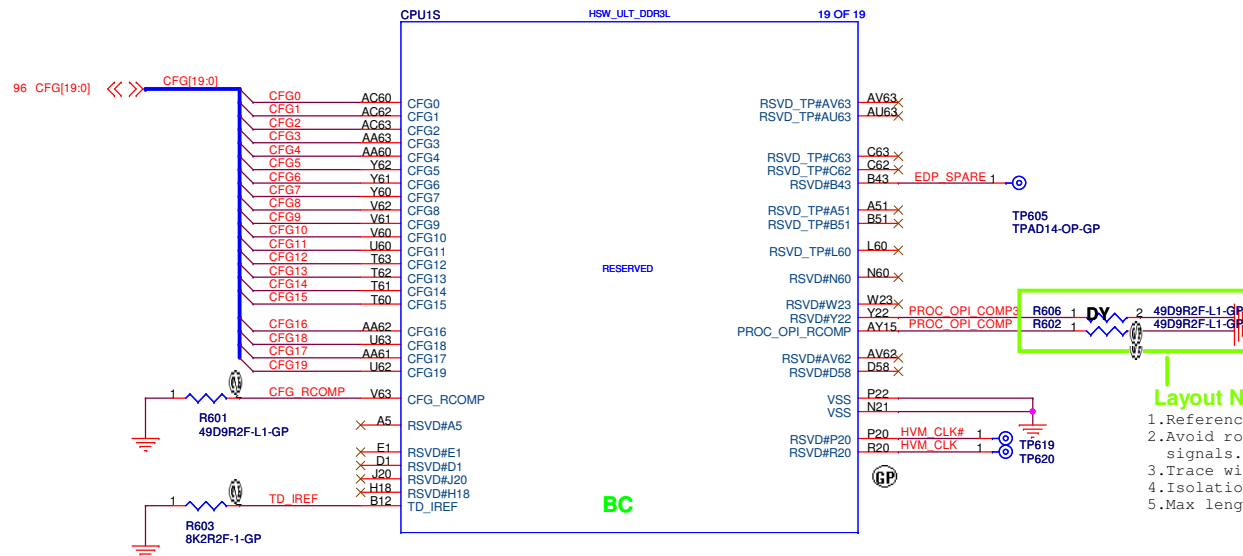


SSID = CPU



Title			
CPU (DDR)			
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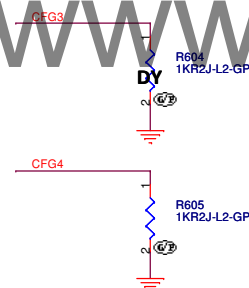
SSID = CPU



Layout Note:

- 1.Referenced "continuous" VSS plane only.
- 2.Avoid routing next to clock pins or noisy signals.
- 3.Trace width: 12~15mil
- 4.Isolation Spacing: 12mil
- 5.Max length: 500mil

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PHYSICAL DEBUG_ENABLED (DFX PRIVACY)

CFG[3] 0 : ENABLED
SET DFX_ENABLED BIT IN DEBUG INTERFACE MSR
1 : DISABLED

DISPLAY PORT PRESENCE STRAP

CFG[4] 0 : ENABLED
AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
1 : DISABLED
NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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CPU (RESERVED)

Size
A3

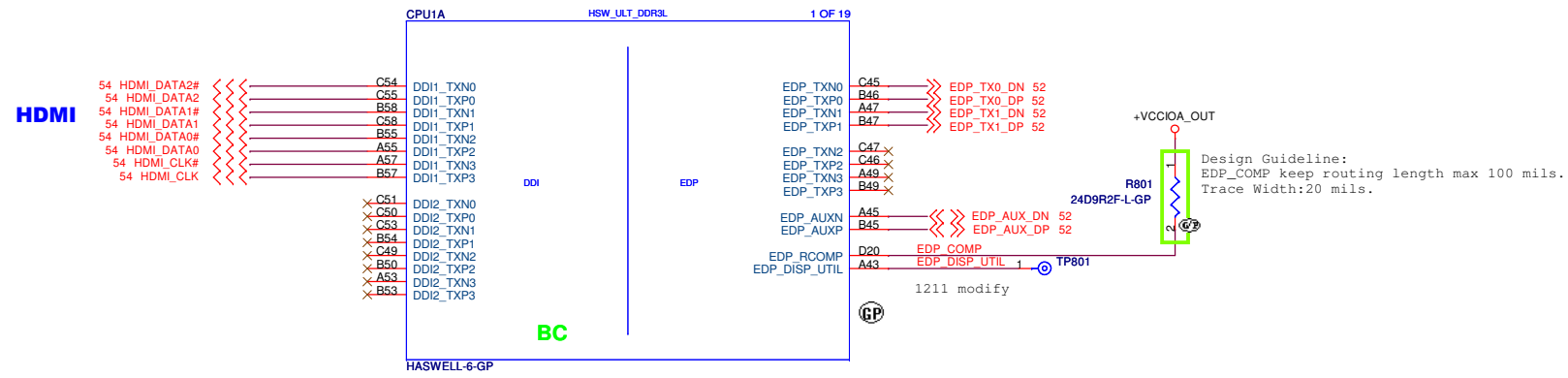
Document Number

Hadley 14"

Rev
A00

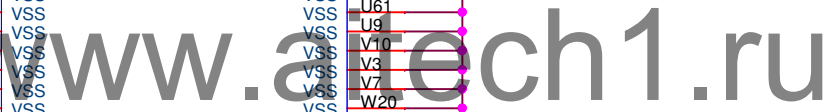
Date: Wednesday, August 14, 2013

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SSID = CPU



1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwngth match<25mil



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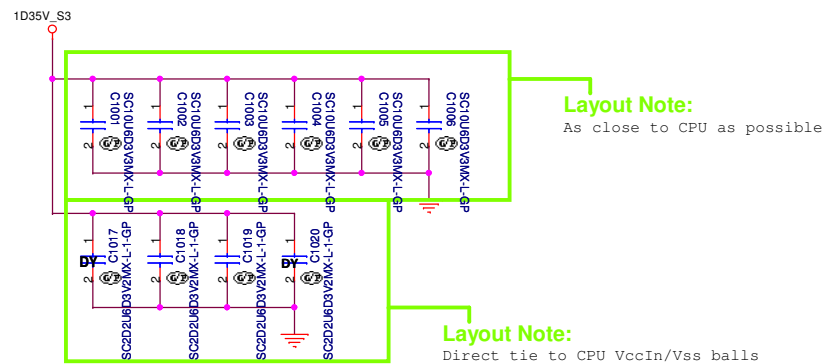
CPU (VSS)

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SSID = CPU



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CPU(Power CAP1)

Size
A3

Document Number

Hadley 14"

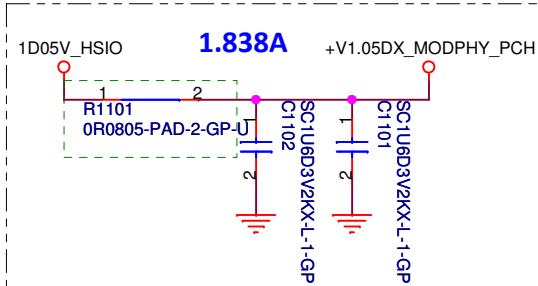
Rev
A00

Date: Wednesday, August 14, 2013

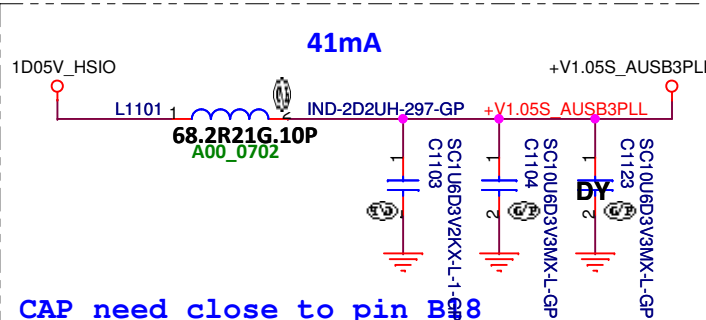
Sheet 10 of 107

SSID = CPU

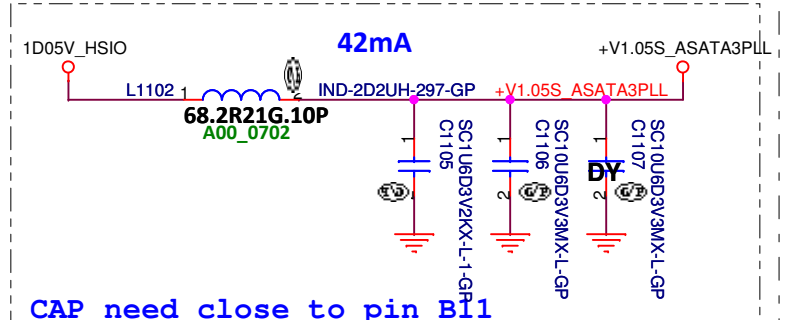
MAX: 1.92A



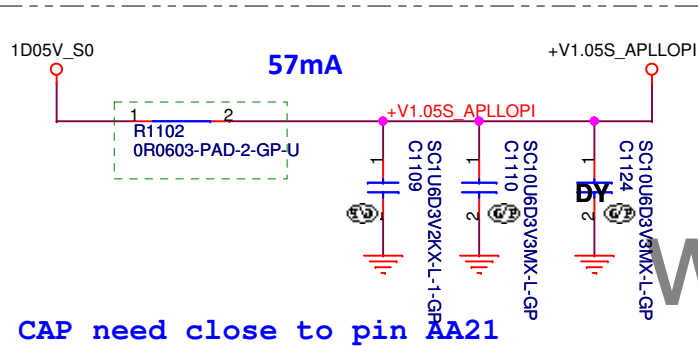
CAP need close to pin K9 L10



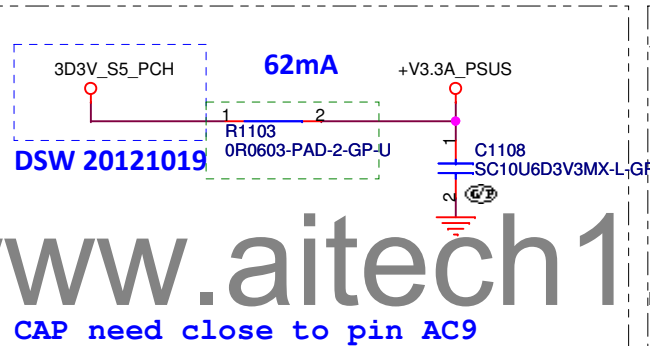
CAP need close to pin B8



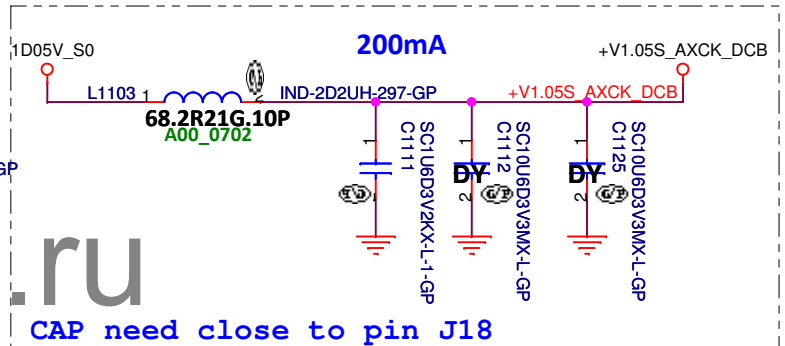
CAP need close to pin B11



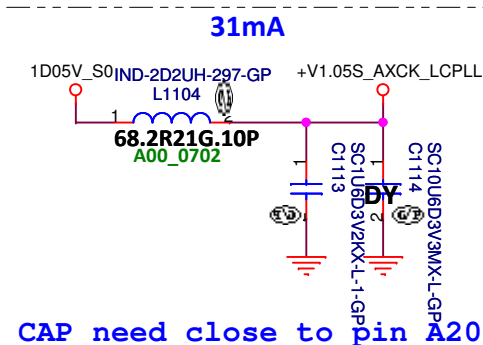
CAP need close to pin AA21



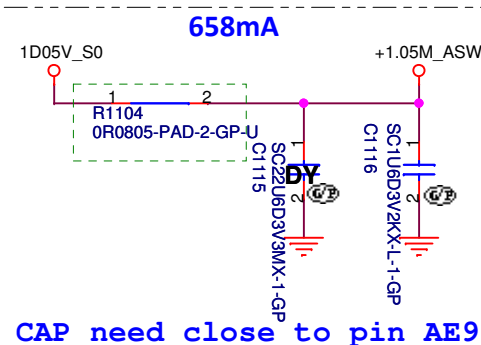
CAP need close to pin AC9



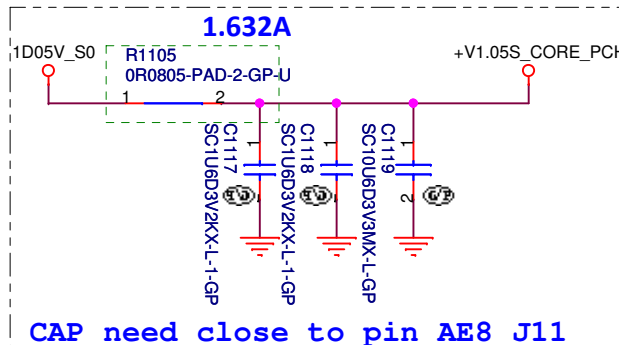
CAP need close to pin J18



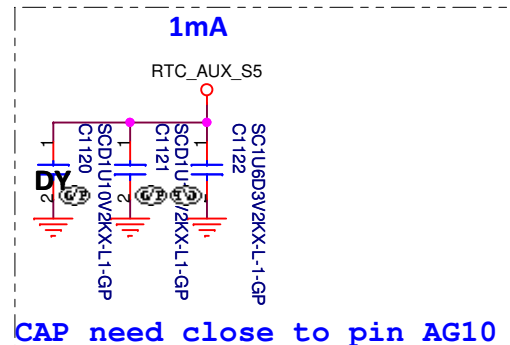
CAP need close to pin A20



CAP need close to pin AE9



CAP need close to pin AE8 J11



CAP need close to pin AG10

X02_0522
Change R1101~ R1105 to short pad

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CPU(Power CAP2)

Size
A4

Document Number

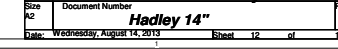
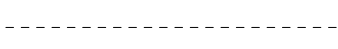
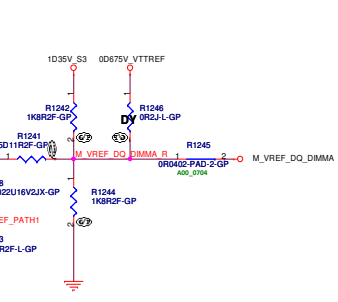
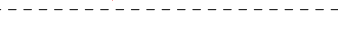
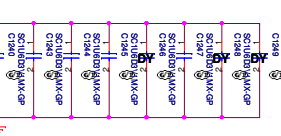
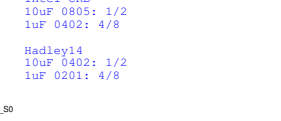
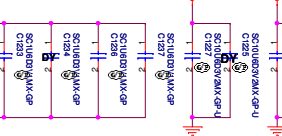
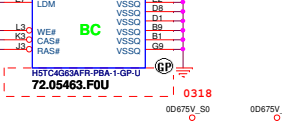
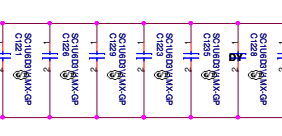
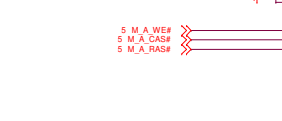
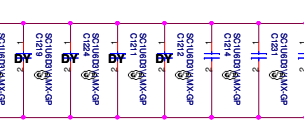
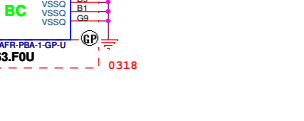
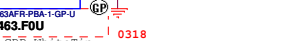
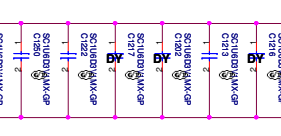
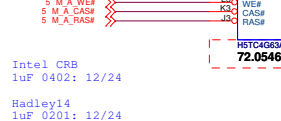
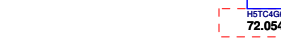
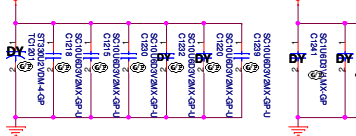
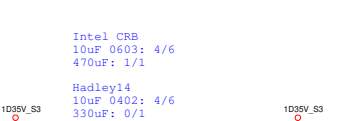
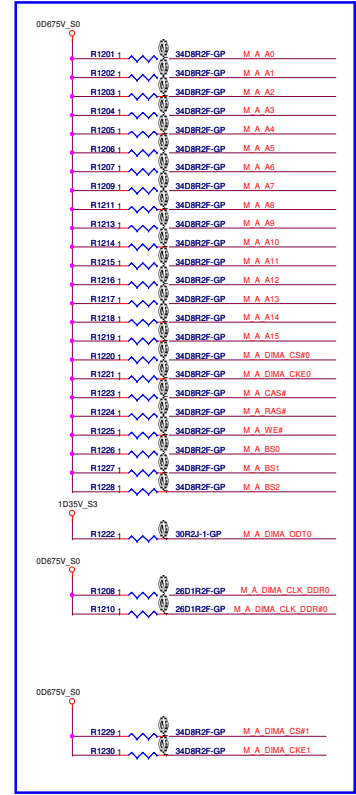
Hadley 14"

Rev
A00

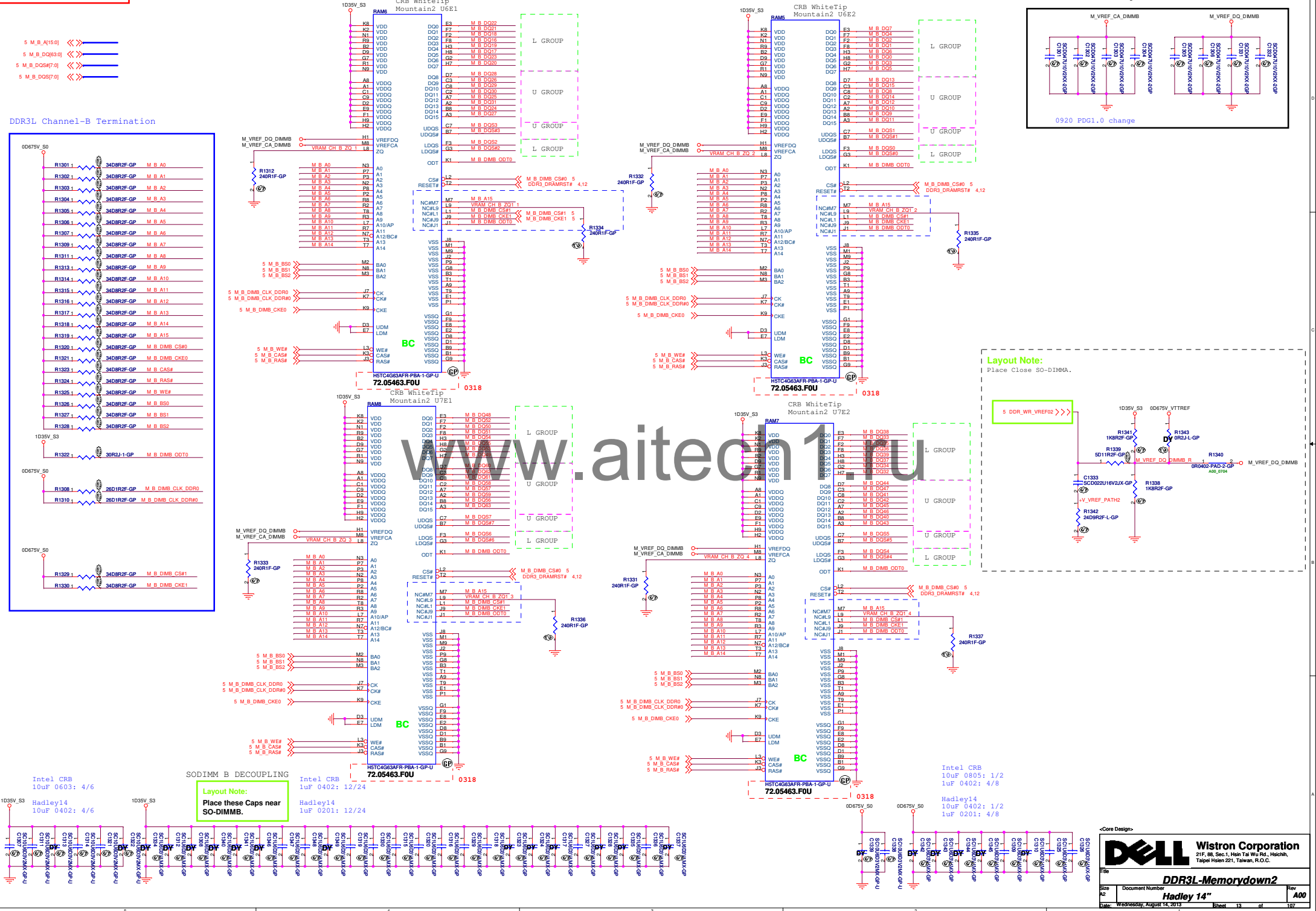
Date: Wednesday, August 14, 2013

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5 M_A_A[15:0] << >>
5 M_A_DQ[63:0] << >>
M_A_DQS#[7:0] << >>
5 M_A_DQS[7:0] << >>




SSID = MEMORY



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M1&M3

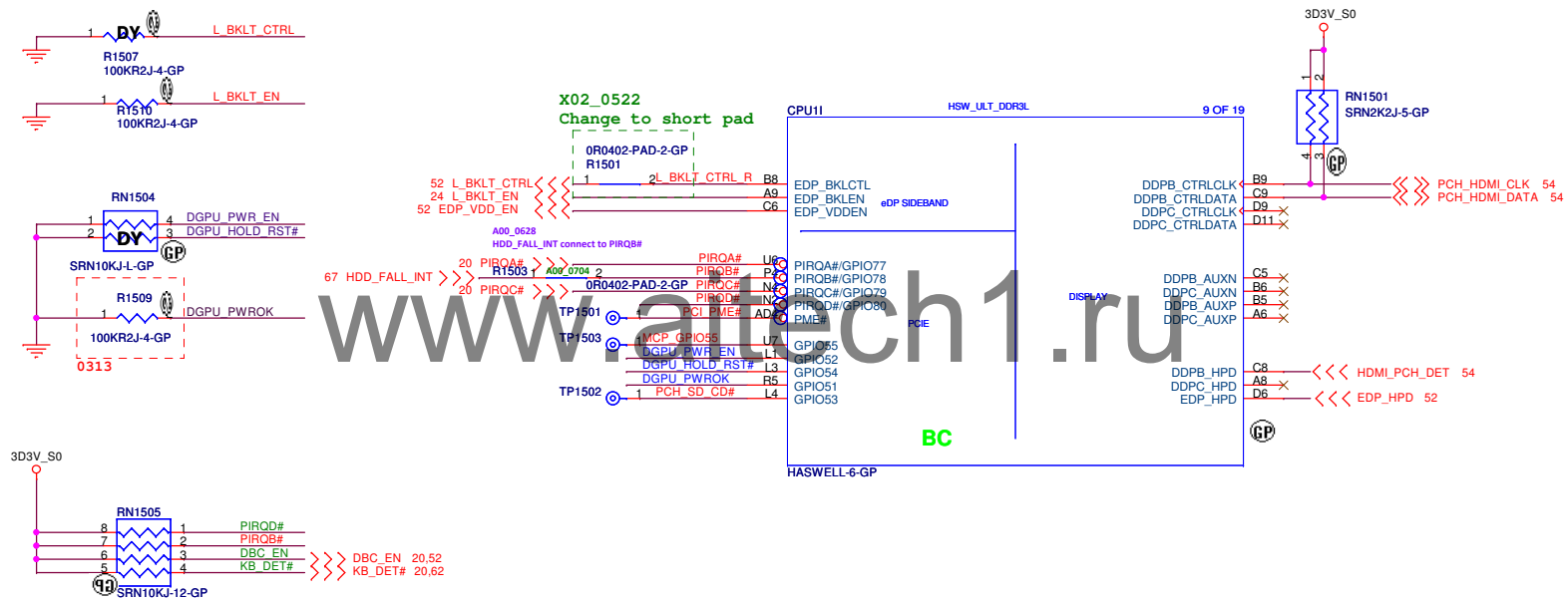
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Rev

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SSID = CPU



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CPU (EDP SIDEBAND/GPIO/DDI)

Size

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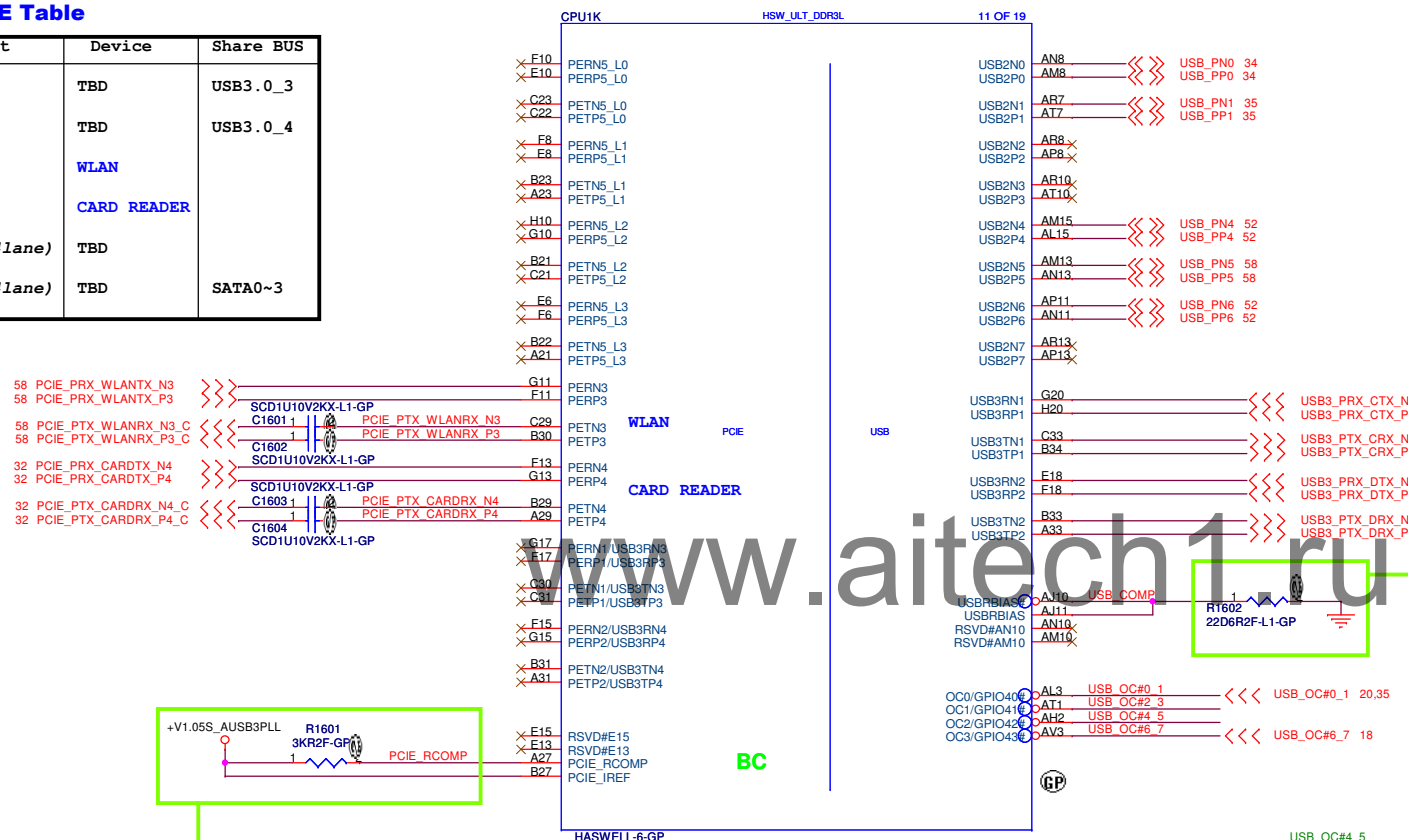
SSID = CPU

PCIE Table

Port	Device	Share BUS
1	TBD	USB3.0_3
2	TBD	USB3.0_4
3	WLAN	
4	CARD READER	
5 (4lane)	TBD	
6 (4lane)	TBD	SATA0~3

USB 2.0 Table

Pair	Device
0	USB3.0 Port2
1	USB3.0 port1 (with Power Share)
2	NC
3	NC
4	CAMERA
5	WLAN
6	Touch Panel
7	NC



- **Layout Note:**

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil



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Title

CPU (PCIe/USB)Size
A

Document Number

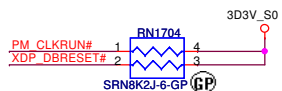
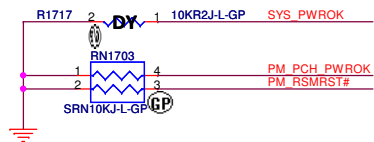
Hadley 14"

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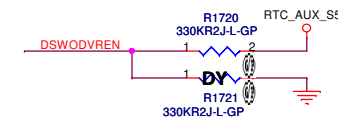
Sheet 16 of 107

SSID = CPU

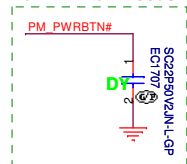


PCH strap pin:

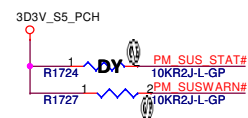
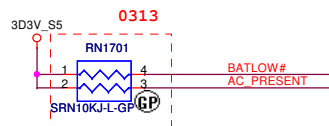
On Die DSW VR Enable	
DSWODVREN	Low = Disable ★ High = Enable (default)



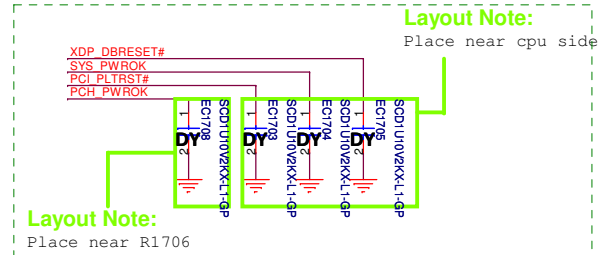
X02_0520
For I7 ESD issue



Layout Note:
Place near CPU

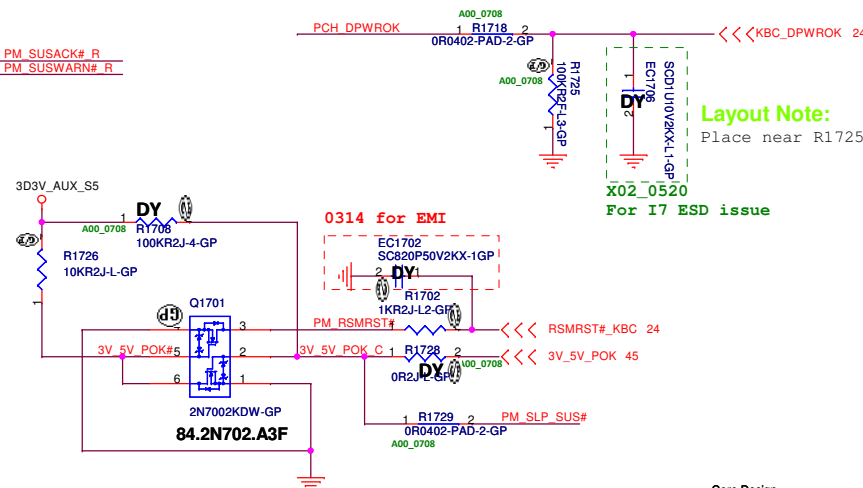


X02_0520
For I7 ESD issue



Layout Note:
Place near R1706

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Layout Note:
Place near R1725

X02_0520
For I7 ESD issue

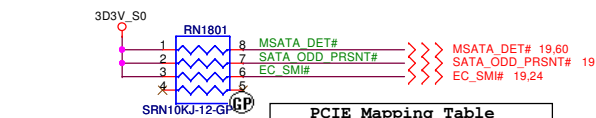
<Core Design>



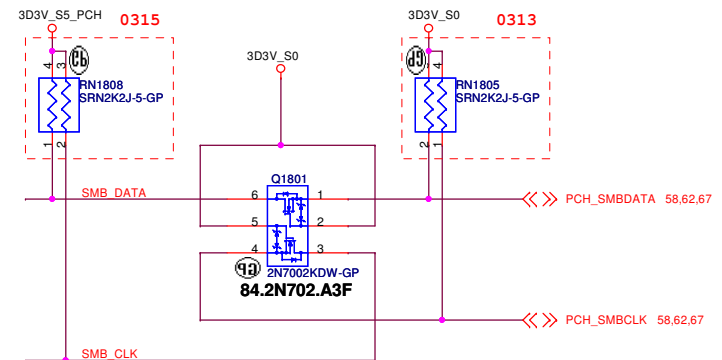
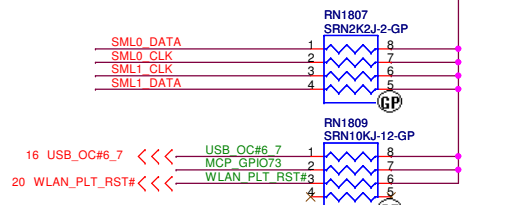
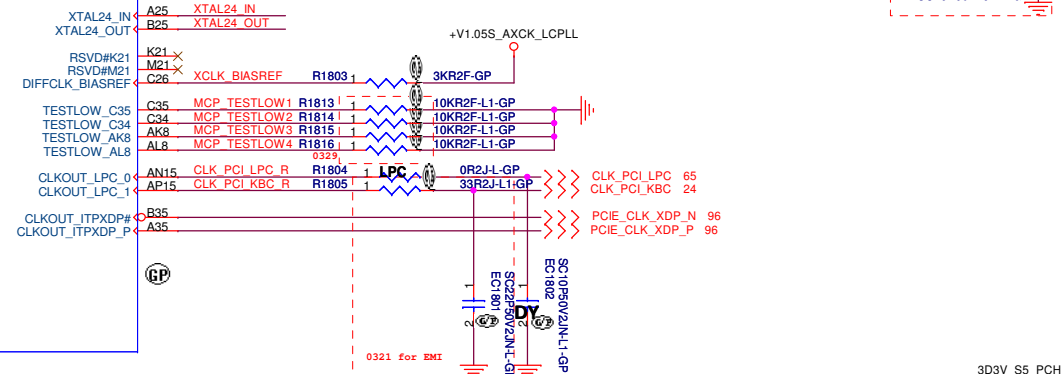
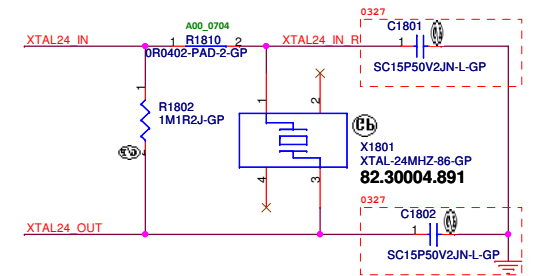
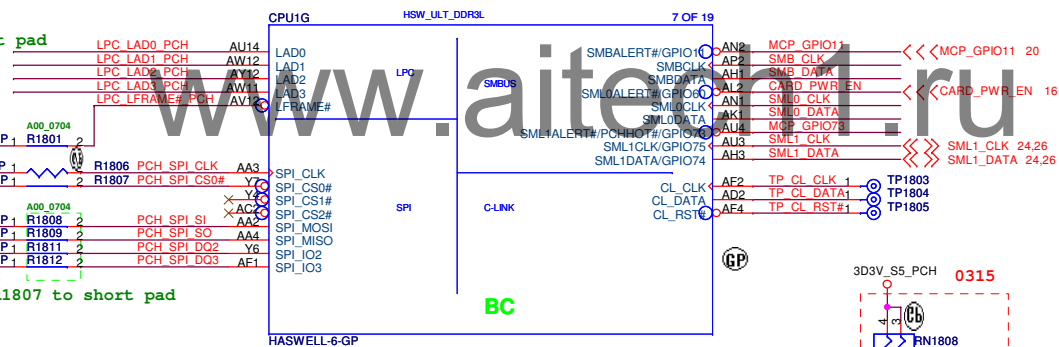
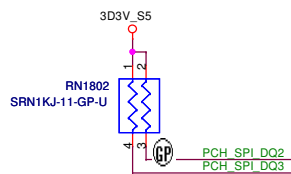
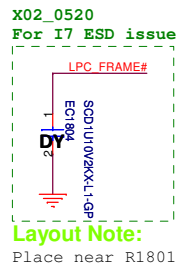
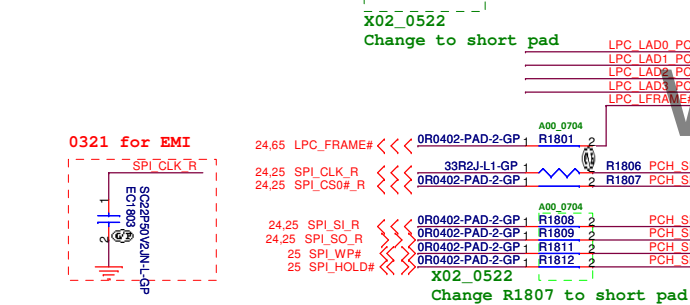
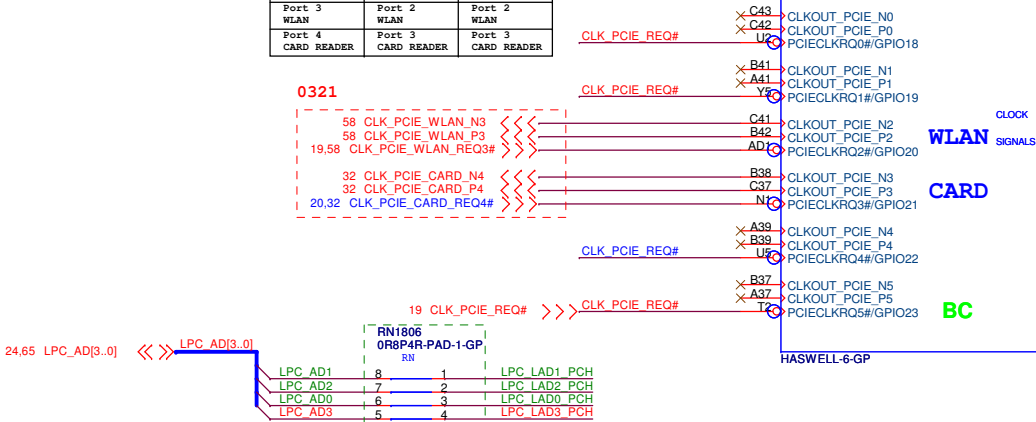
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SSID = CPU



PCIE Port	PCIE CLK	REQ#
Port 3 WLAN	Port 2 WLAN	Port 2 WLAN
Port 4 CARD READER	Port 3 CARD READER	Port 3 CARD READER



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CPU (CLK/SMB/LPC/SPI)

Size

Document Number

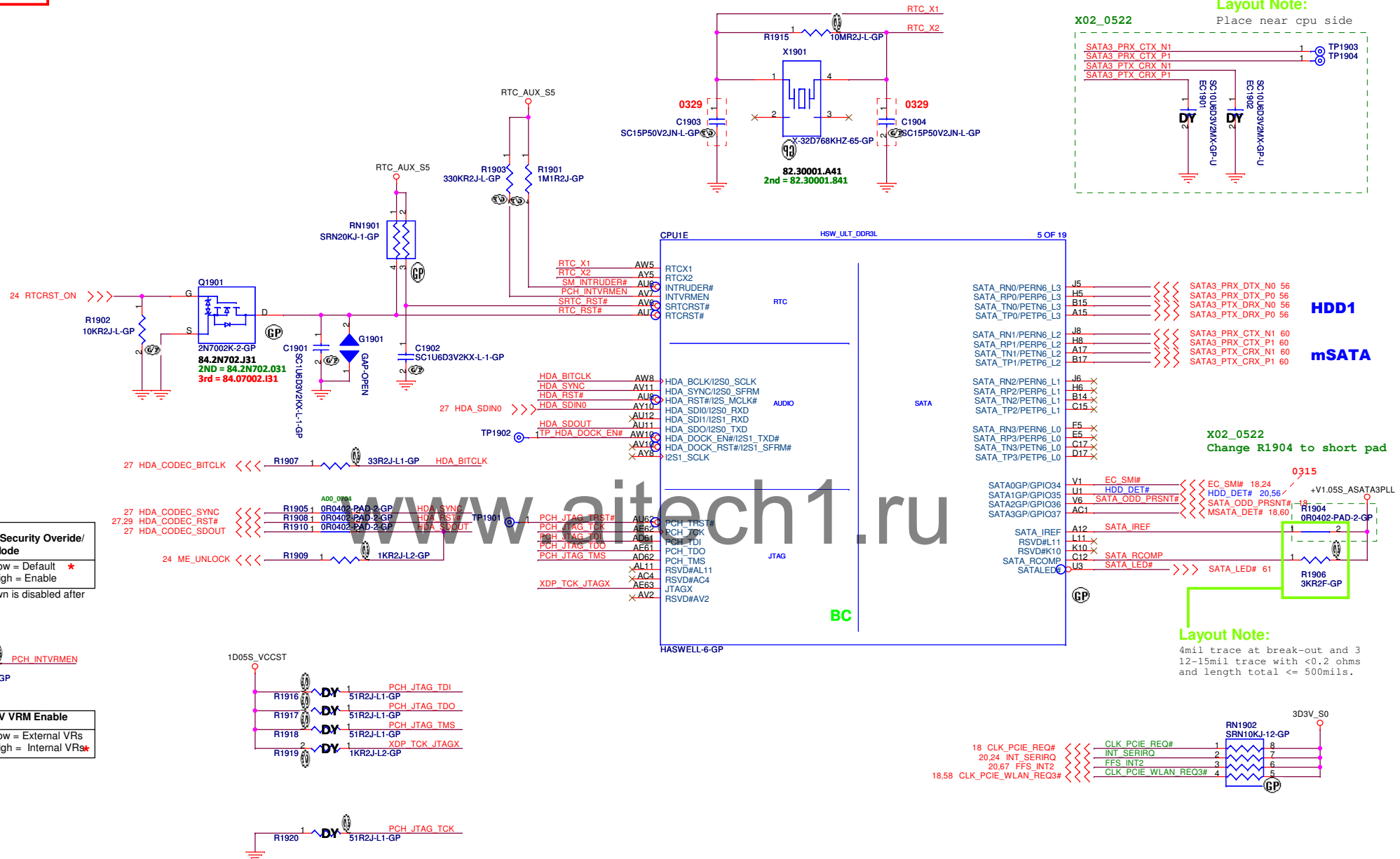
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SSID = CPU



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Title

CPU (RTC/SATA/HDA/JTAG)

Size
A

Document Number

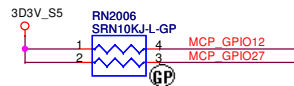
Hadley 14"

Rev
A00

Date: Wednesday, August 14, 2013

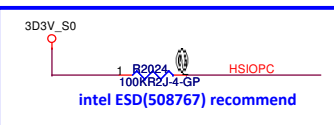
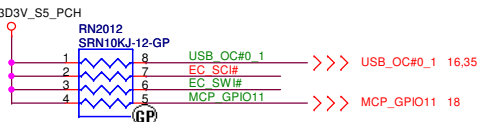
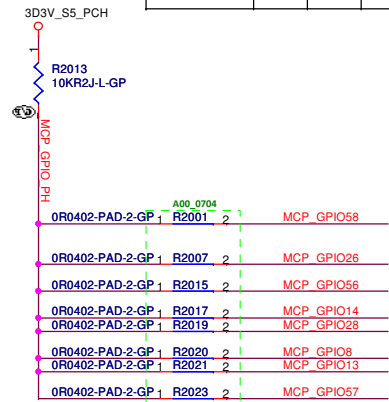
Sheet 19 of 107

SSID = CPU



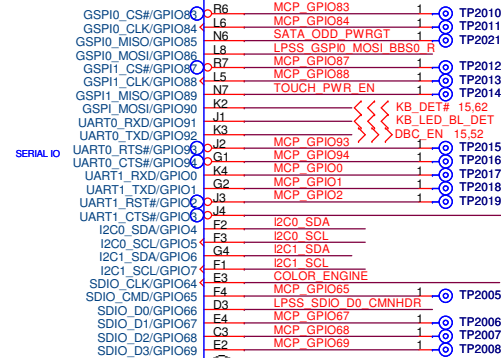
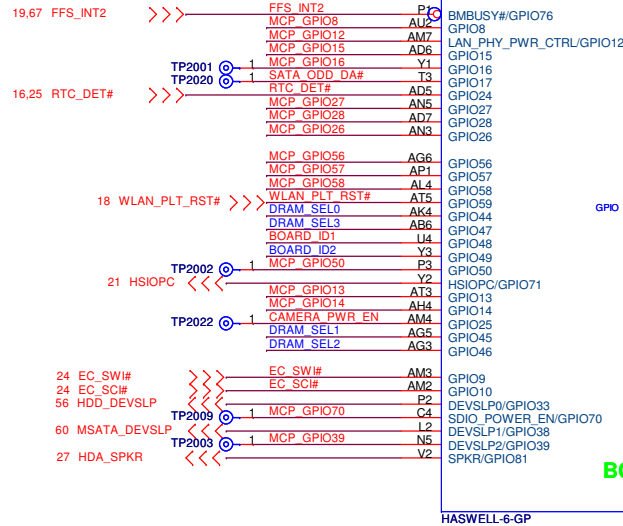
SSI Memory Matrix Table

Vendor	Size	M53 GPIO47	M52 GPIO46	M51 GPIO45	M50 GPIO44
Hynix	4	0	0	0	0
Hynix	6	0	0	0	1
Hynix	8	0	0	1	0
Samsung	4	0	0	1	1
Samsung	6	0	1	0	0
Samsung	8	0	1	0	1
Micron	4	0	1	1	0
Micron	6	0	1	1	1
Micron	8	1	0	0	0
Hydley 15/17 SODIMM	1	1	1	1	1



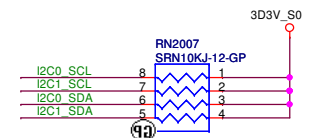
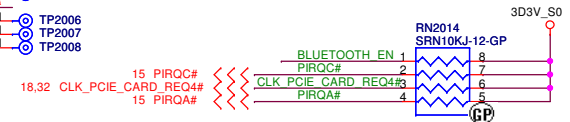
BIOS strap pin:

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
PX(AMD)	0	0
DIS	0	1
UMA	1	0
Optimus(NV)	1	1

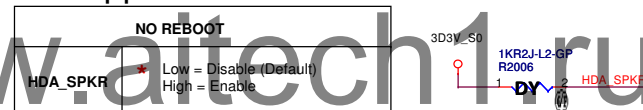


Layout Note:

- 1.Referenced "continuous" VSS plane only.
- 2.Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PCH strap pin:



The internal pull-down is disabled after PLTRST# deasserts

it is for "A1" stepping.

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	<p>★ Low = Disable "Top-Block swap" mode (Default)</p> <p>High = Enable "Top-Block swap" mode</p>

The internal pull-down is disabled after PLTRST# deasserts

Need SW double confirm if that's needed Top-Block swap

TLS Confidentiality	
GPIO15	<p>★ Low = Disable Intel ME Crypto TLS</p> <p>High = Enable Intel ME Crypto TLS</p>

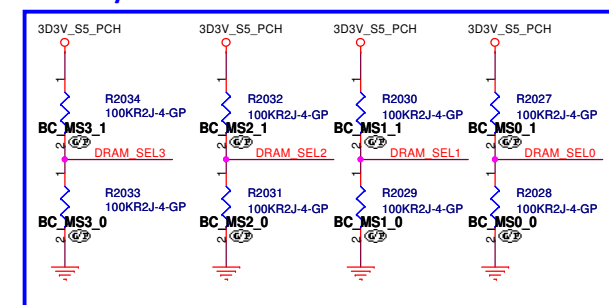
The internal pull-down is disabled after RSMRST# deasserts.

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

Memory Matrix Define



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<Core Design>

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Title _____

CPU (GPIO)

Size	Document Number	Rev
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A3	Hadley 14"	A00
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Date: Wednesday, August 14, 2013 Sheet 20 of 107

SSID = CPU



PT : stuff R2122 ,DY R2114(reserve HSIO SW for check function)
(All High Speed enter sleep mode, HSIO SW will be turn off)



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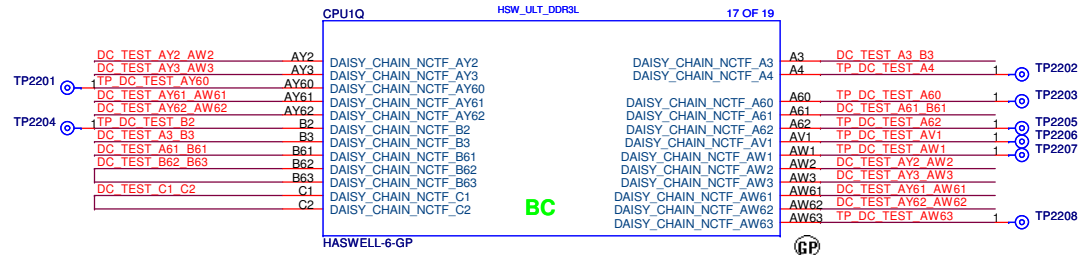
CPU (POWER2)

Hadley 14"

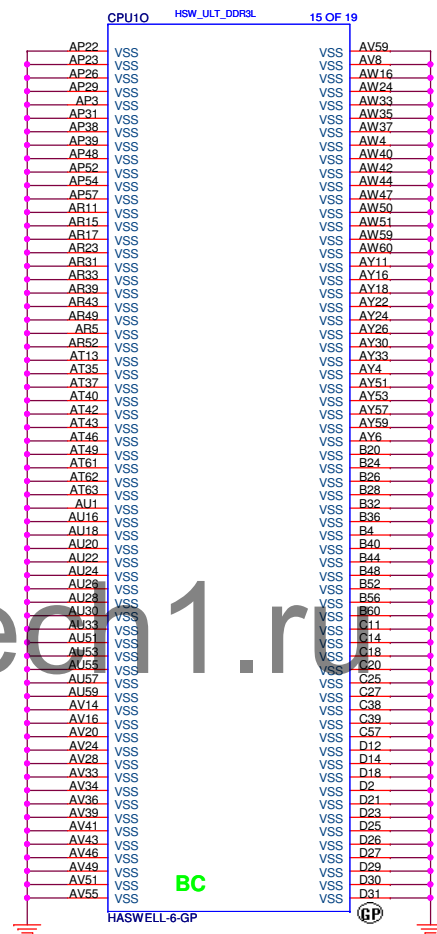
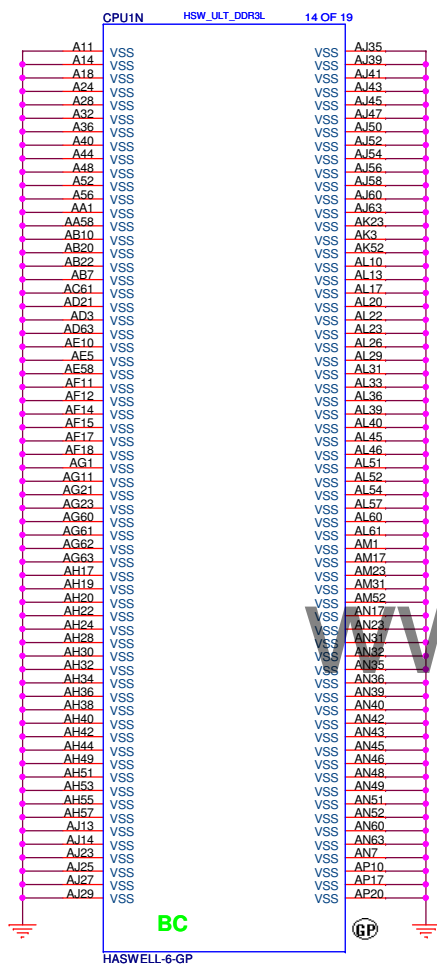
Rev
A00

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SSID = CPU

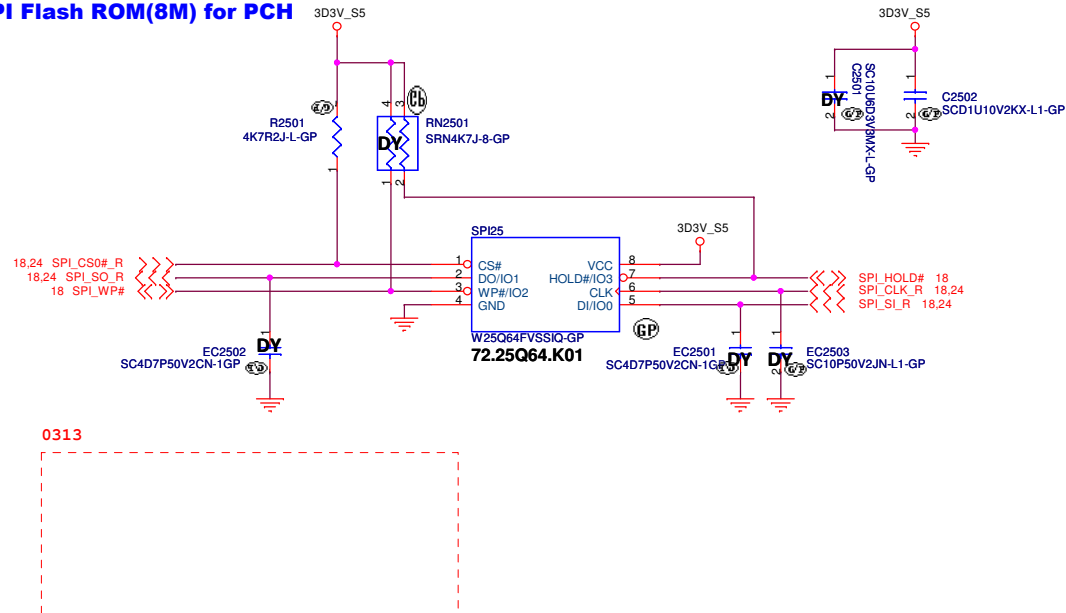


SSID = CPU

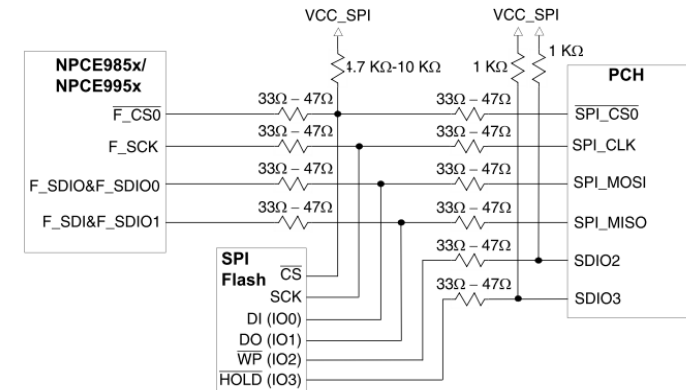


SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



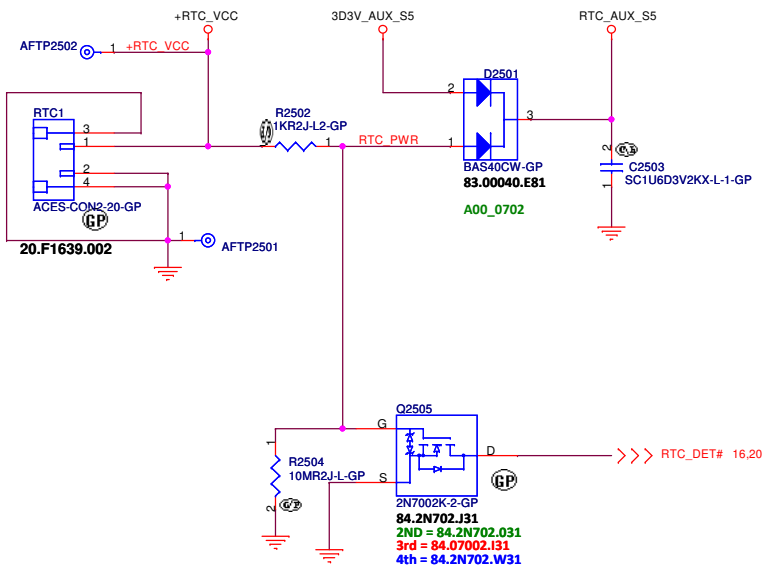
Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

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SSID = RBATT



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Title

Flash/RTC

Size
A3

Document Number

Hadley 14"

Date: Wednesday, August 14, 2013

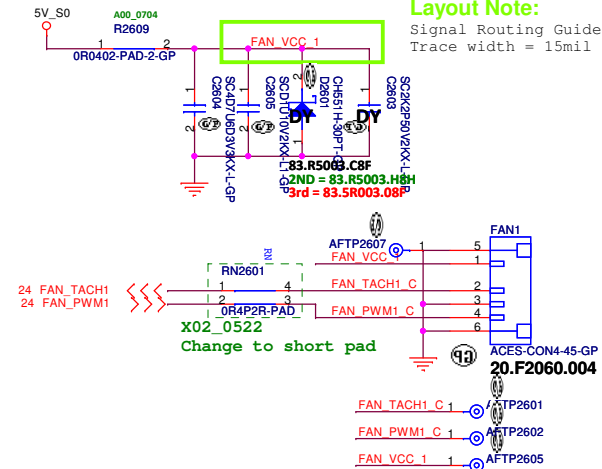
Sheet 25 of 107

Rev
A00

SSID = Thermal

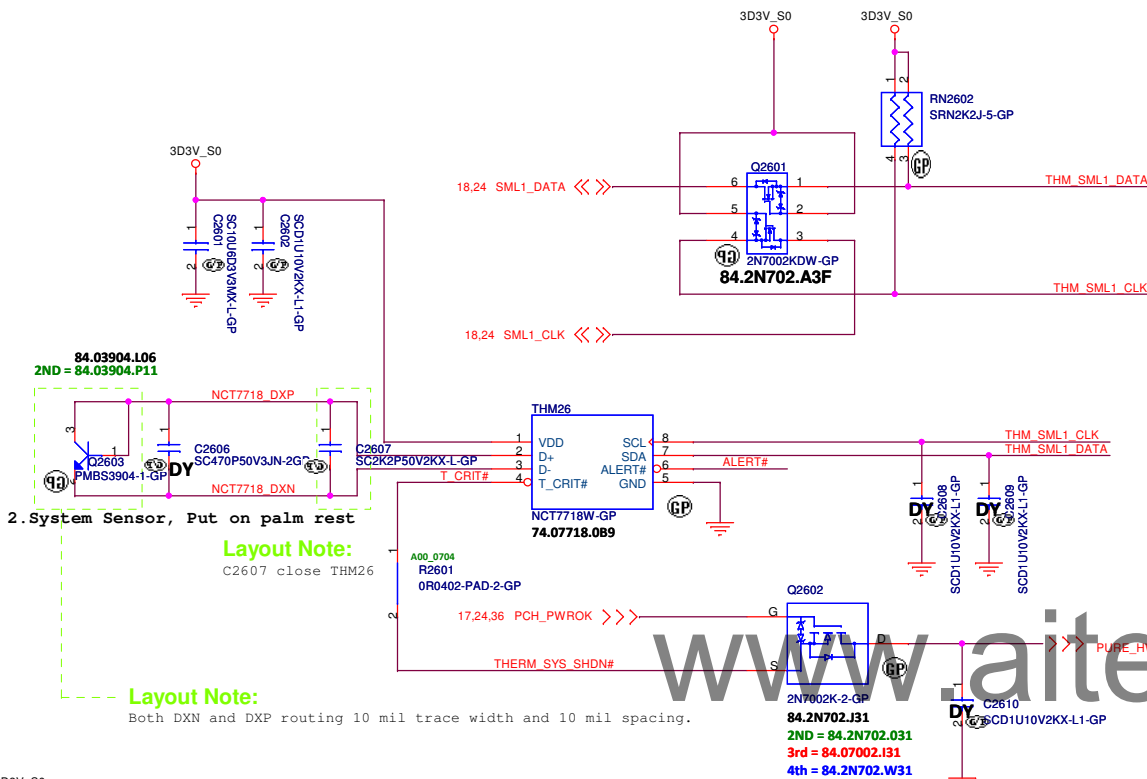
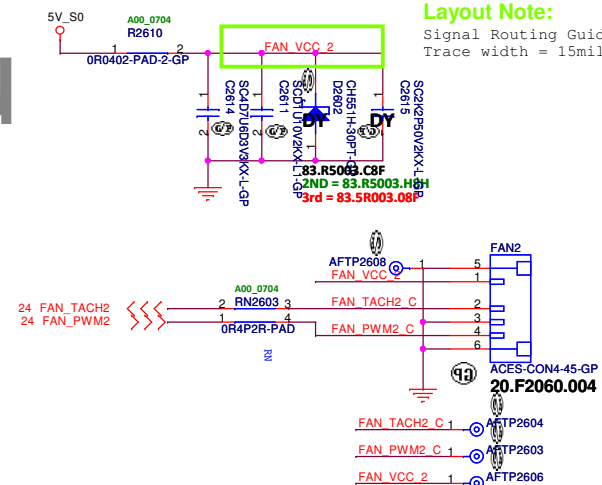
PWM FAN1

Signal Routing Guideline:
Trace width = 15mil



PWM FAN2

Signal Routing Guideline:
Trace width = 15mil



C2607 close THM26

C2607 close THM26

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



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Title

Thermal NCT7718W/Fan

Size

Document Number

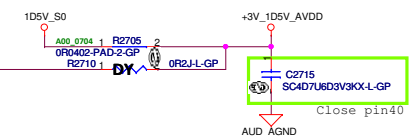
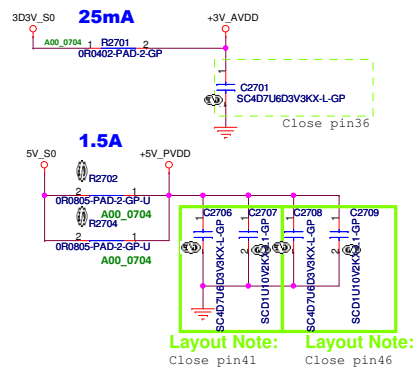
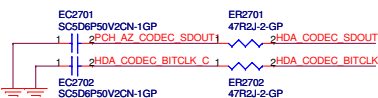
Hadley 14

Date: Wednesday, August 14, 2013

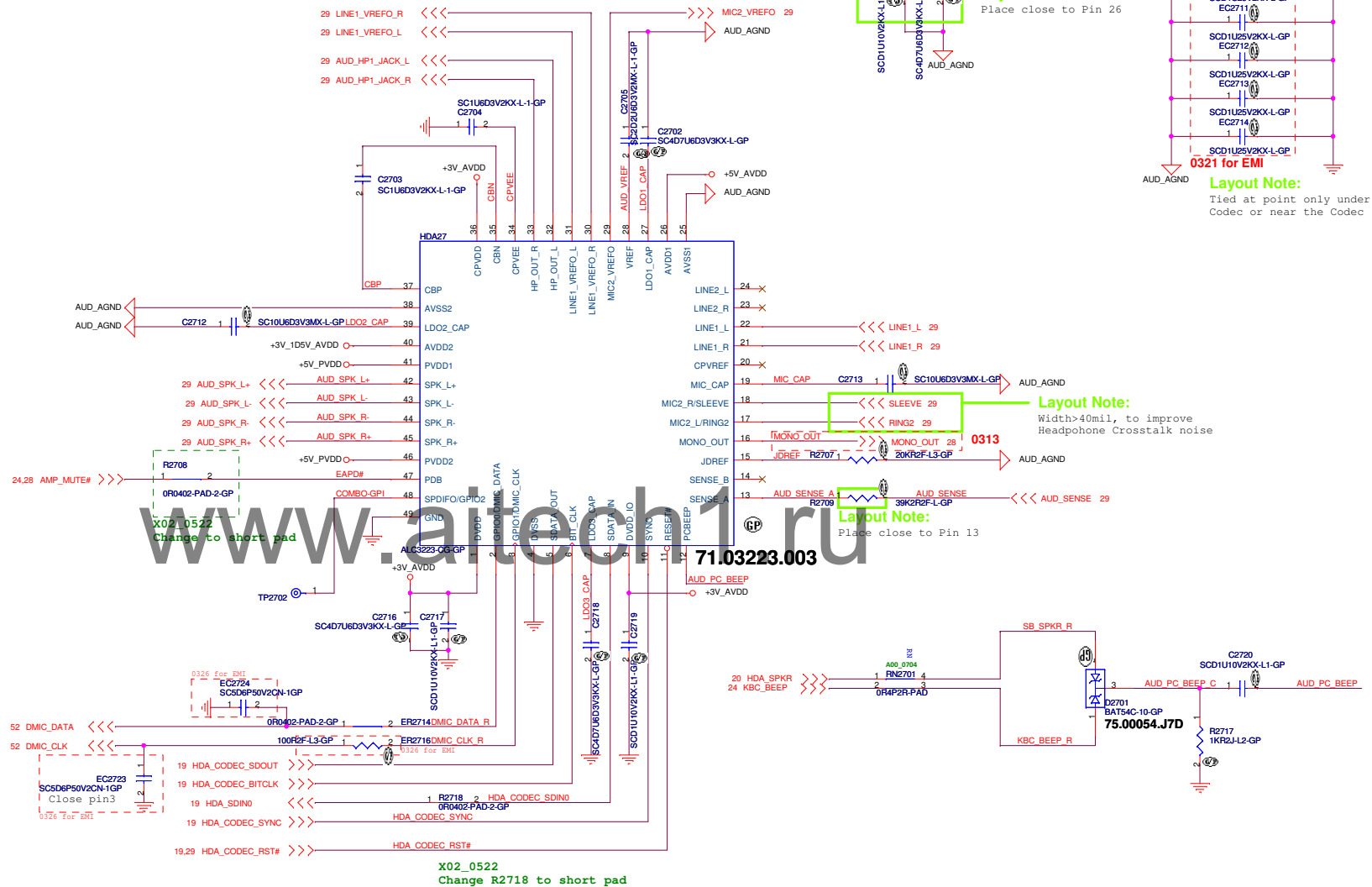
Sheet 26 of 107

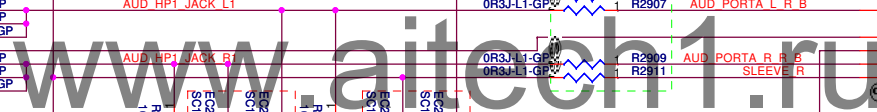
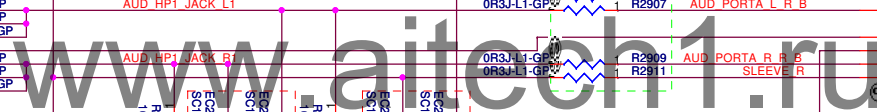
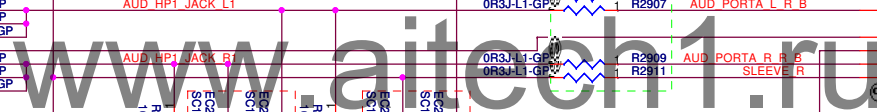
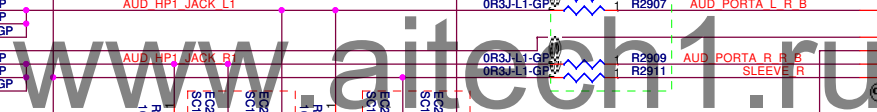
Rev	A00
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SSID = AUDIO

**Azalia I/F EMI**

X02_0527
Change EC2723, EC2724, EC2701, EC2702
to 5.6pF for RF request






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<Core Design>



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Title

Reserved

Size
A3

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Hadley 14"


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Title

Reserved

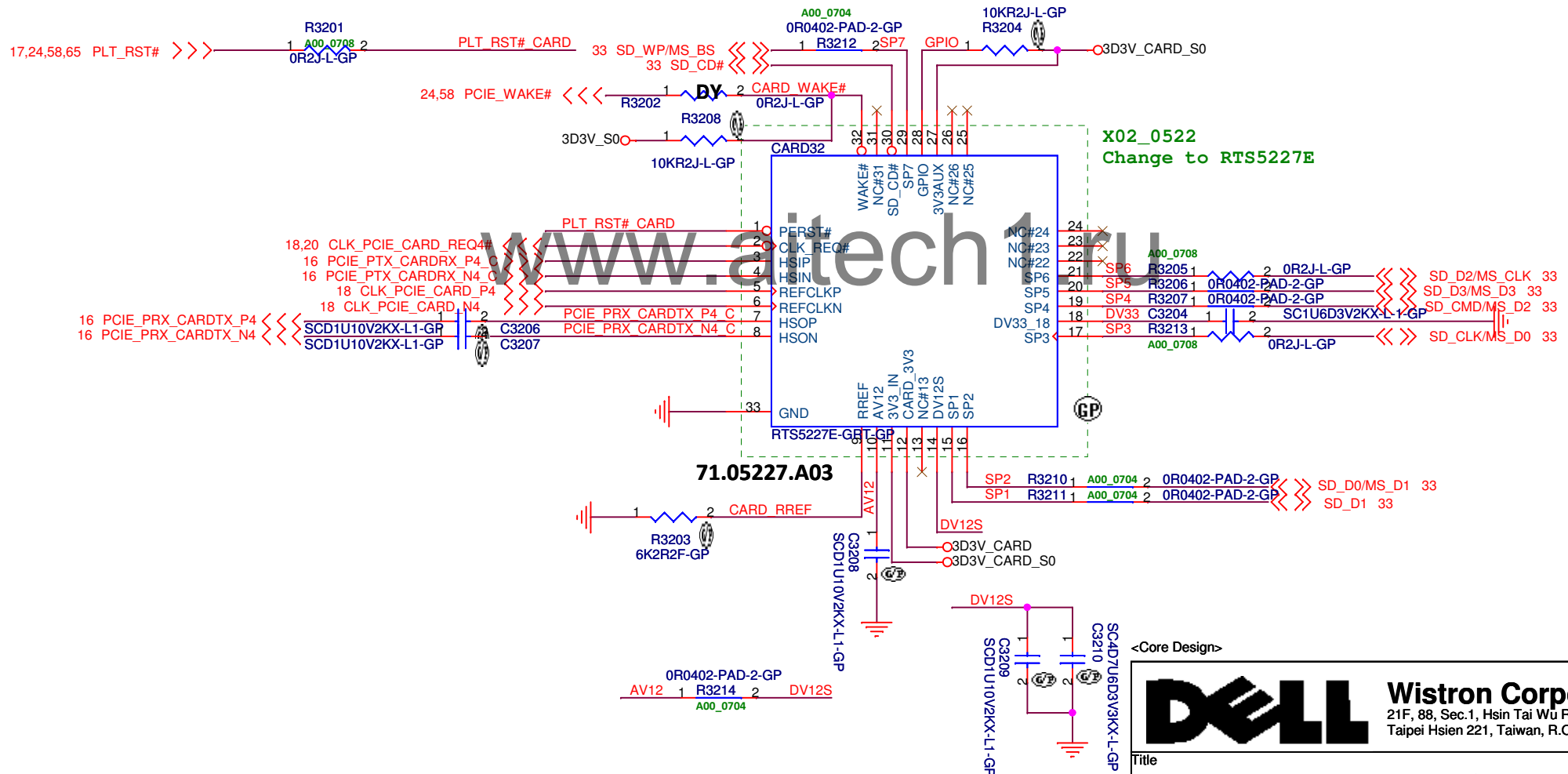
Size	Document Number	Rev
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SSID = SDIO

Remove Switch(No support D3 cold)

Layout Note:
closed to pin27



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Title

Card Reader(RTS5227E)

Size

Document Number

Rev

Hadley 14"

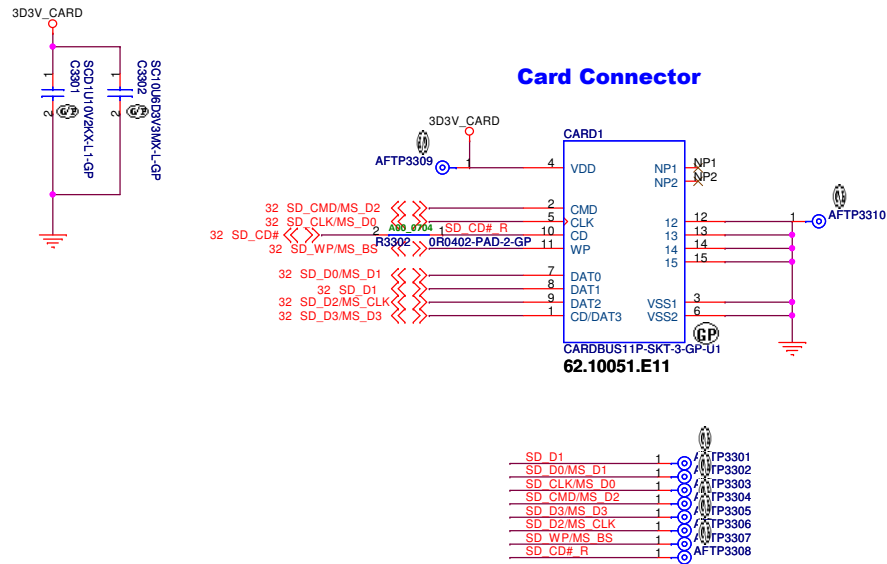
A00

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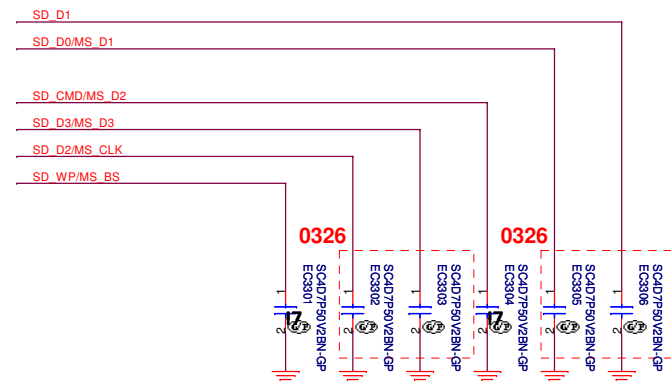
SSID = SDIO



Layout Note:

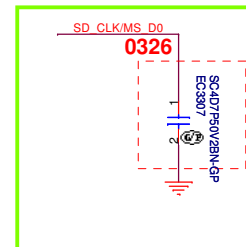
Close to Card Reader CONN

For EMI Reserved



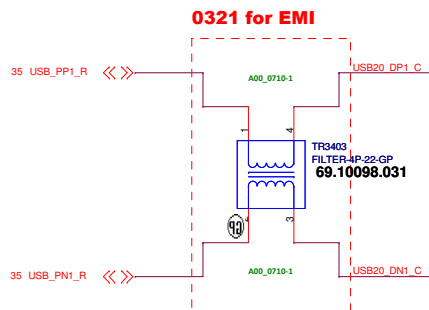
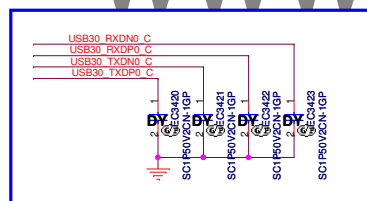
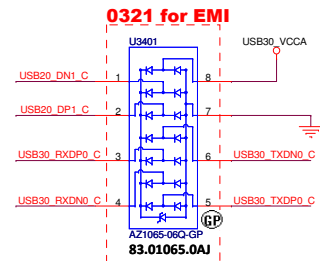
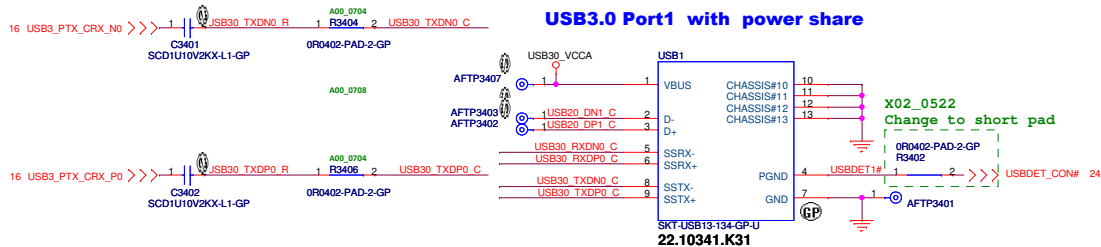
Layout Note:

closed to chip side

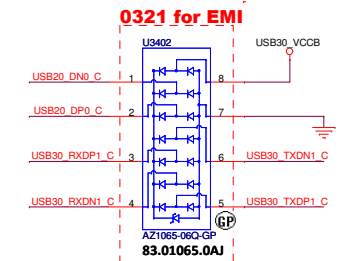
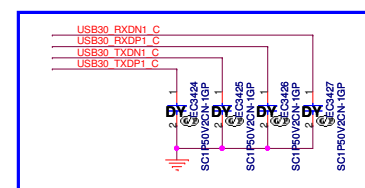
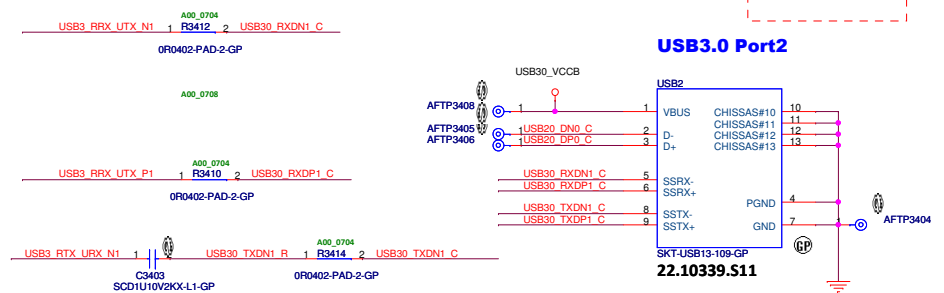
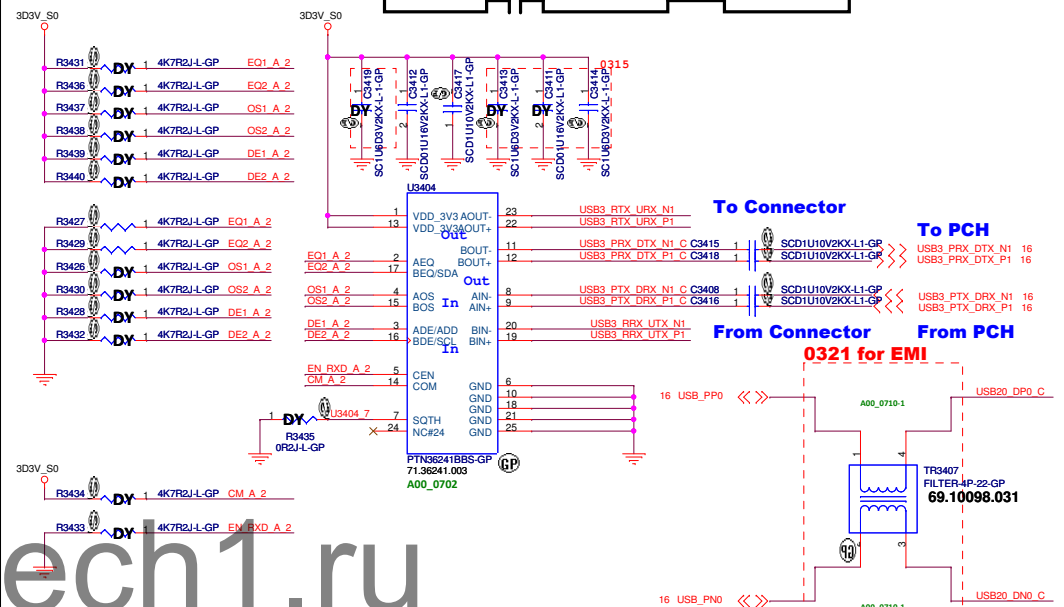


SSID = USB

USB Port1 with power share



USB Port2



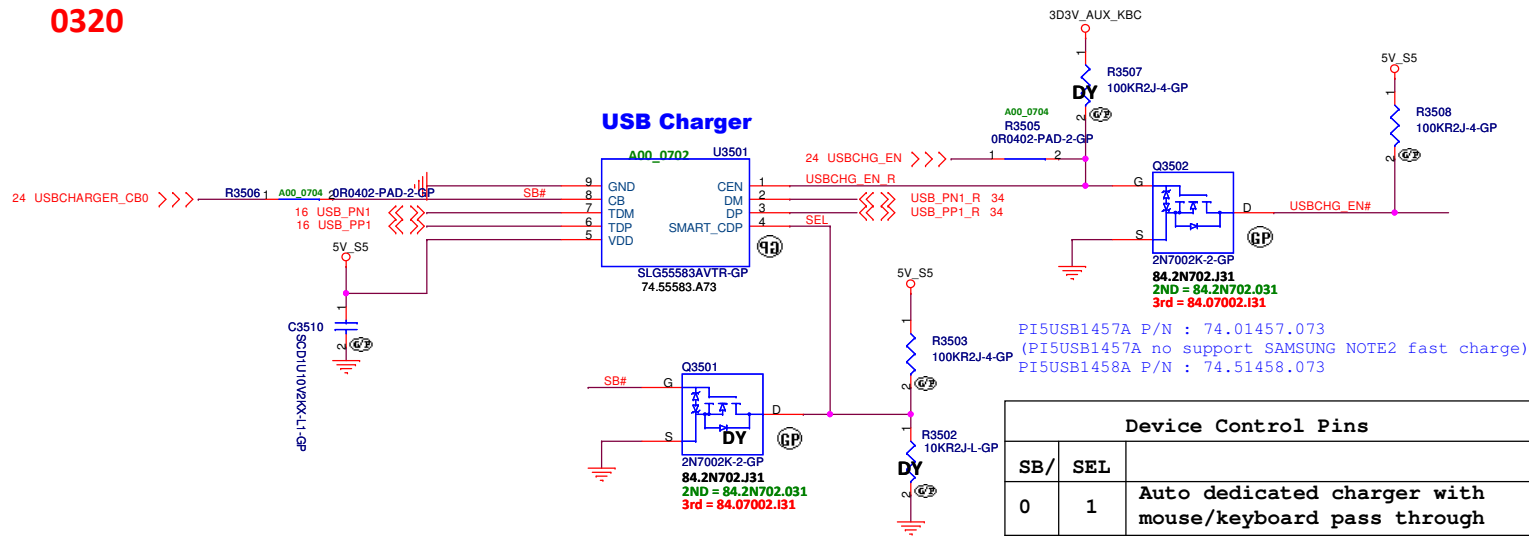
<Core Design>



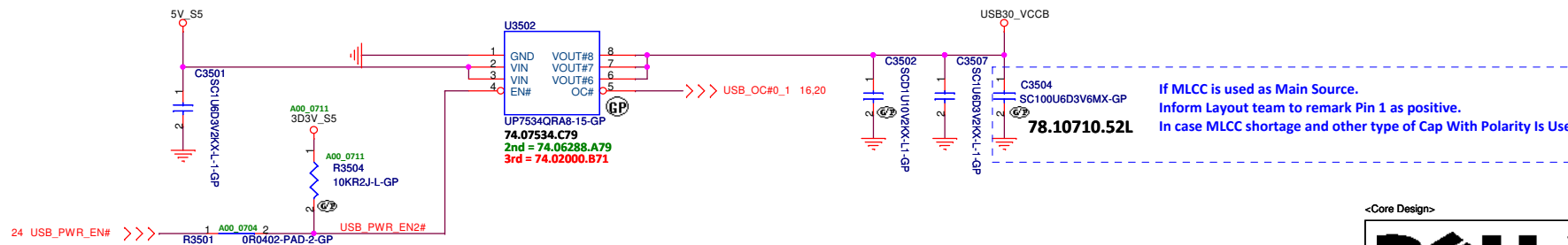
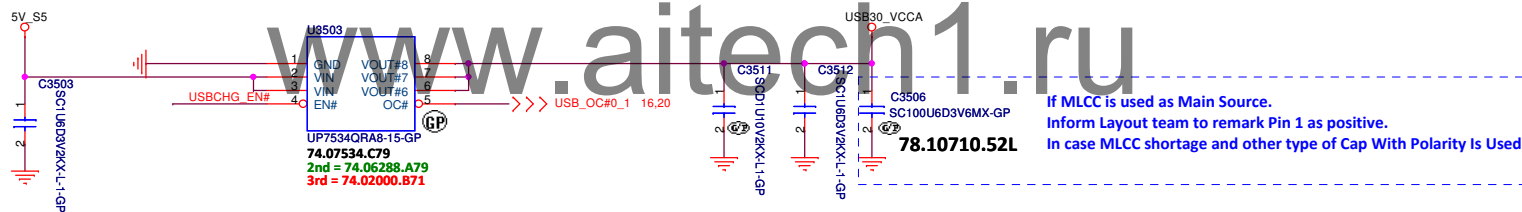
Title			
USB3.0(1)			
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SSID = USB

0320



Device Control Pins		
SB/	SEL	
0	1	Auto dedicated charger with mouse/keyboard pass through
1	1	S0 charging with CDP or SDP only (depending on external device)



ROSA Run Power

Power Good



Power Plane Enable

Hadley 14"

Rev
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SSID = Reset.Suspend

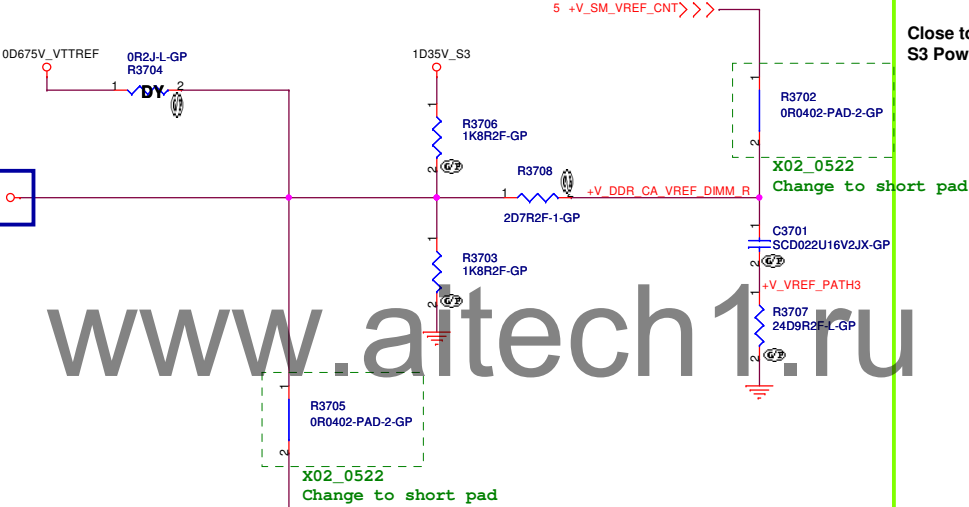
Layout Note:
Place Close SO-DIMMA.

SA_DIMM_VREFDQ
SODIMM1

M_VREF_CA_DIMMA

SB_DIMM_VREFDQ
SODIMM2

M_VREF_CA_DIMMB



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Title

S3 Power Reduction

Size
A3

Document Number

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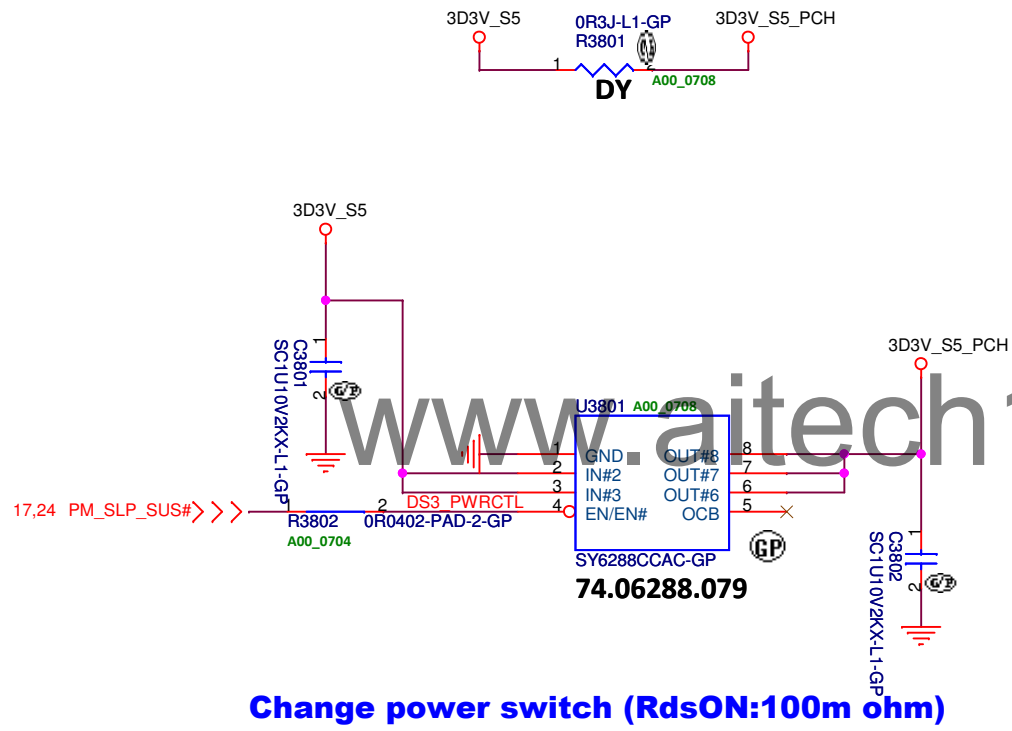
Rev

A00


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SSID = Reset.Suspend




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DSW			
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Title

Reserved


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Title

Size
A3

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Title

Reserved

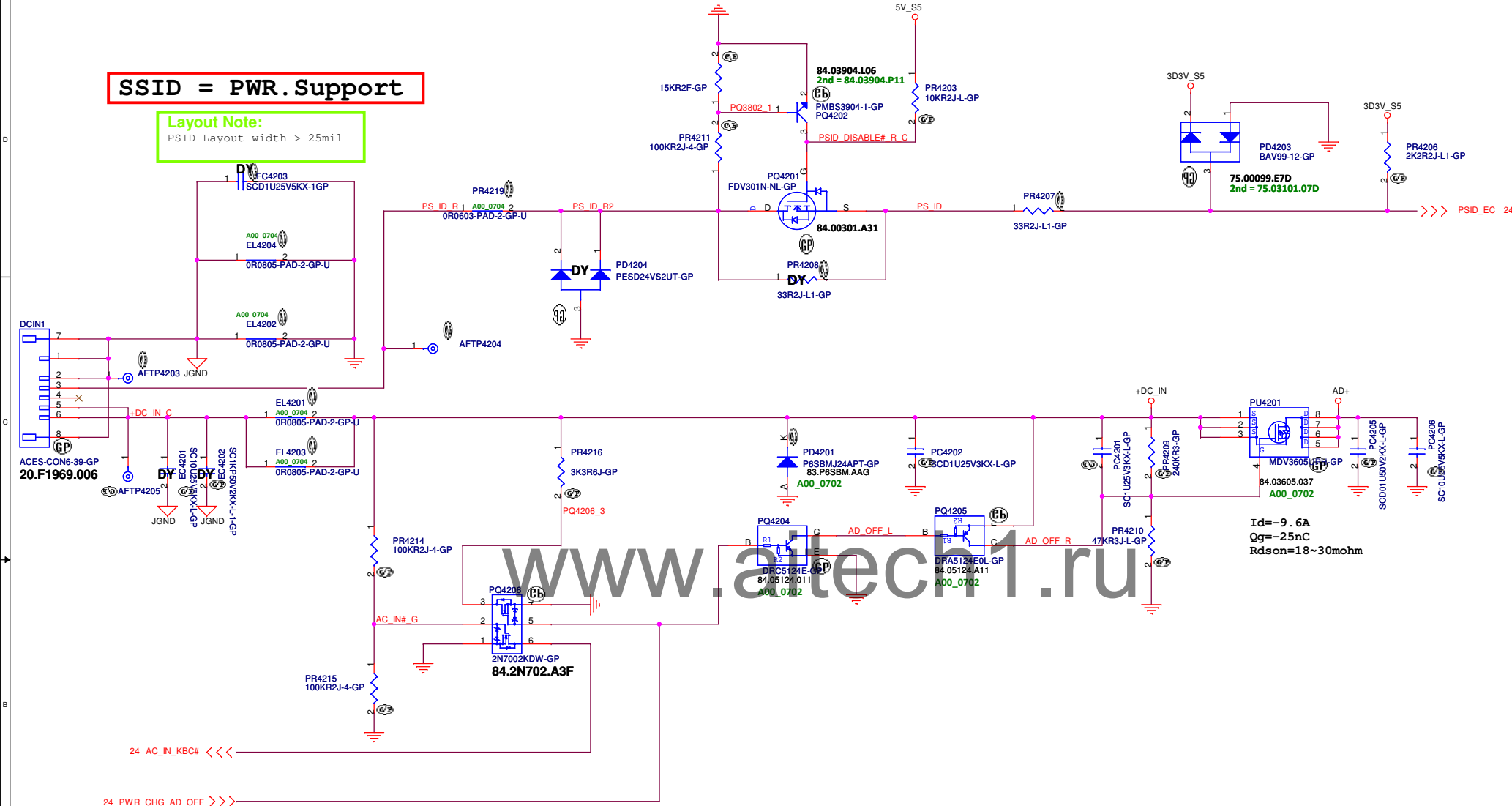
Size	Document Number	Rev
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```
SSID = PWR.Support
```

Layout Note:
PSID Layout width > 25mil

PSID Layout width > 25mil



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Title

DCIN

Size
A3

Document Number

Hadley 14"

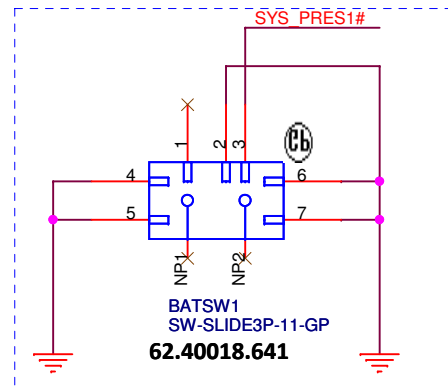
Rev
A00

Date: Wednesday, August 14, 2013

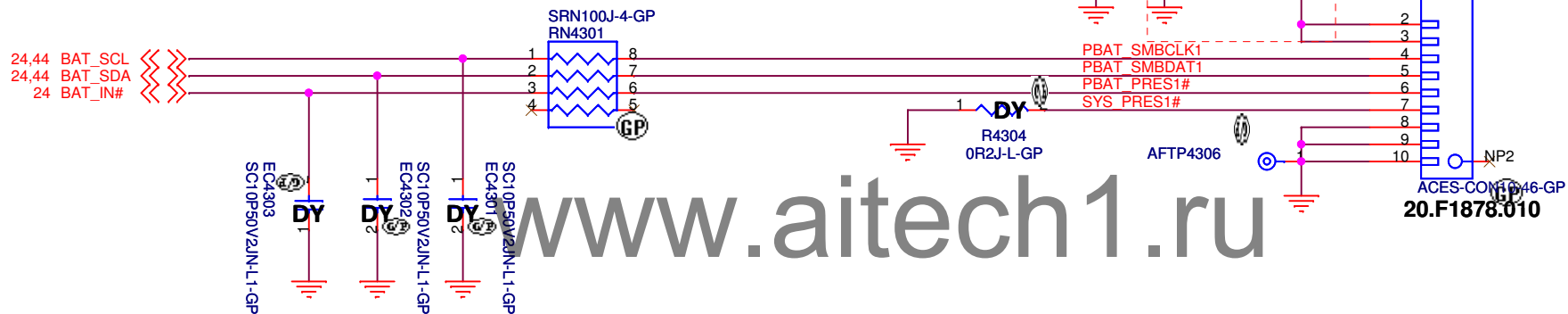
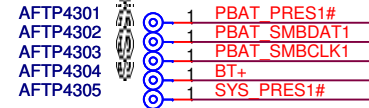
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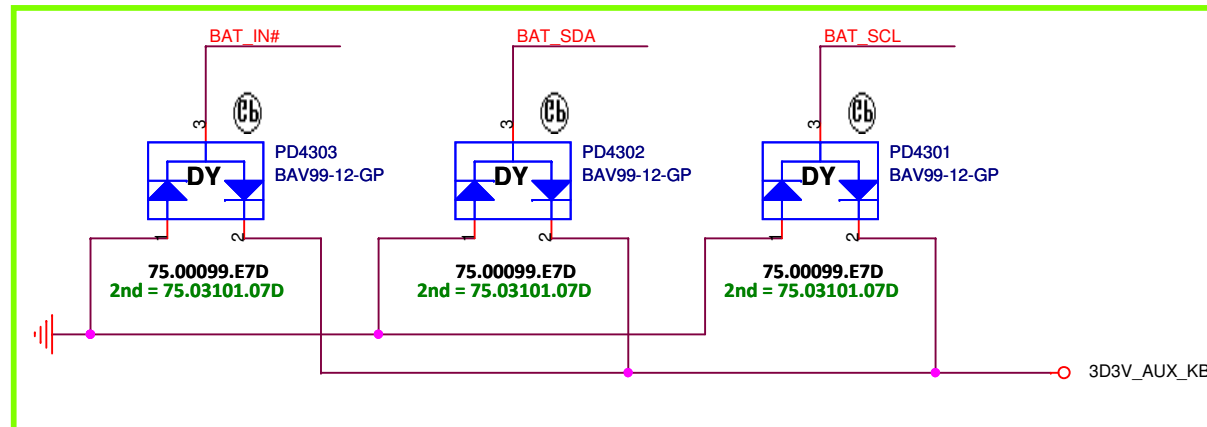
SSID = PWR.Support



If non-removable battery ,
BATSW1 need stuff



Layout Note: Place near Battery CONN



If battery is Detachable ,
PD4301~4303 need stuff

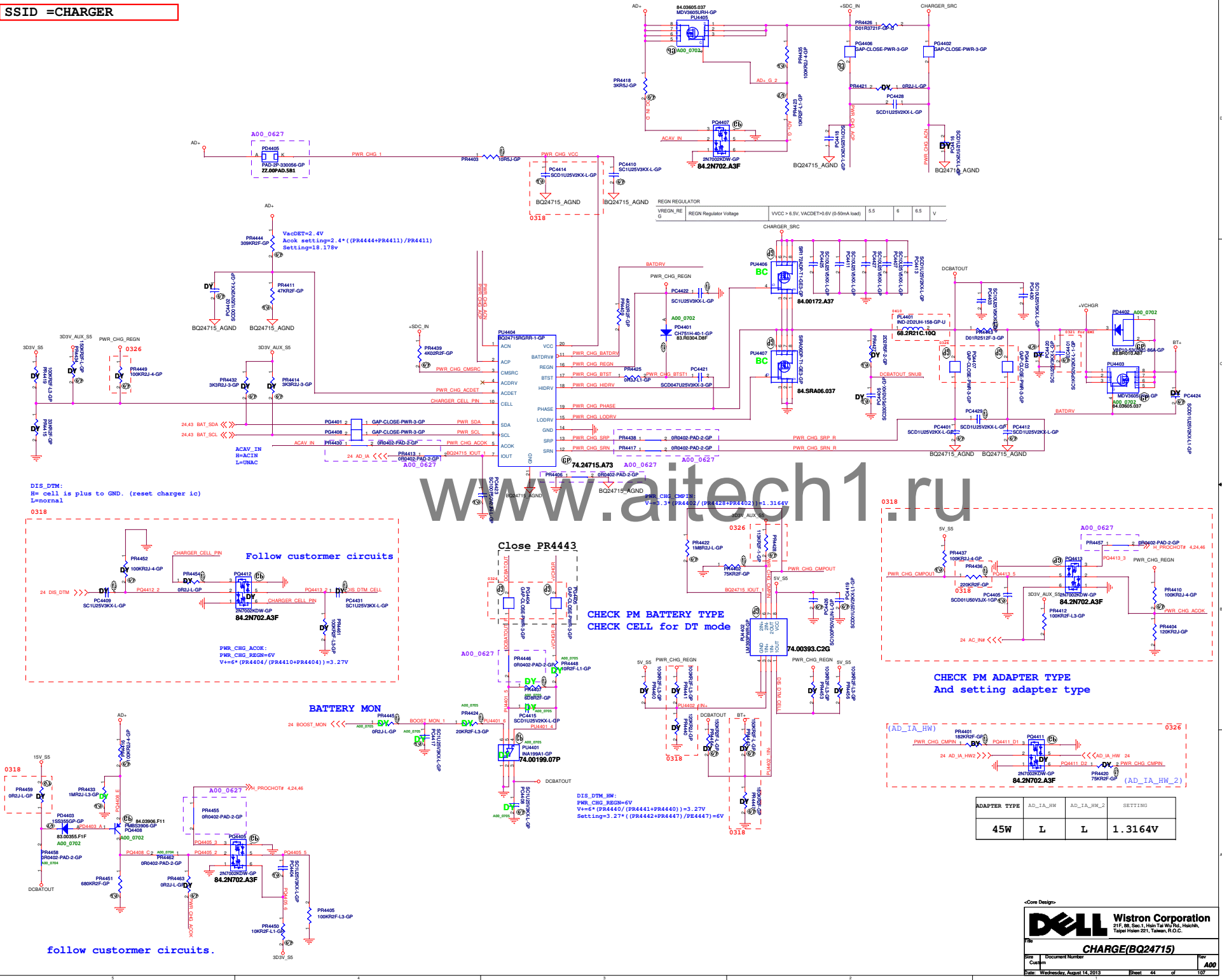
<Core Design>



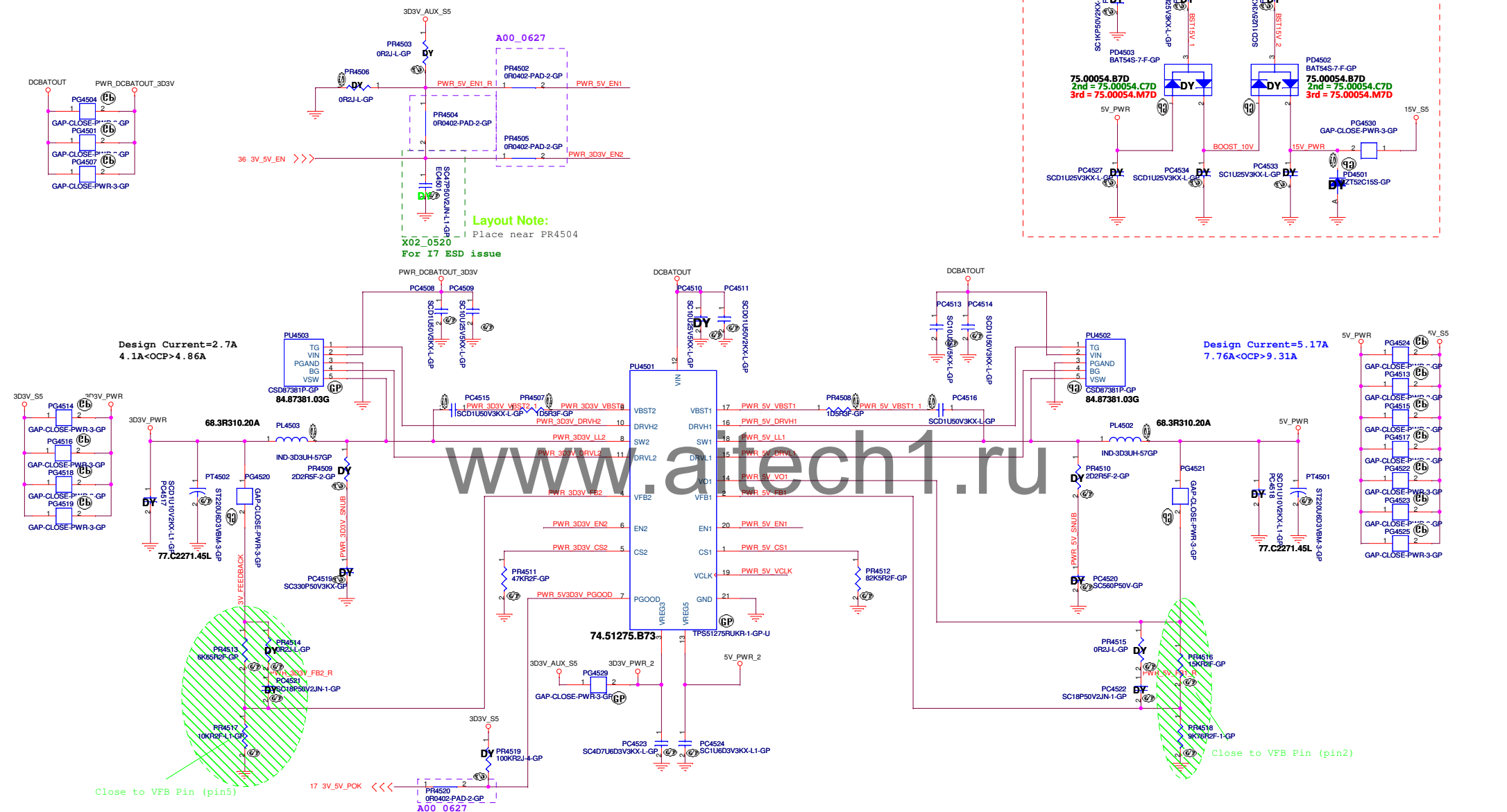
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Title			BATT CONN	
Size A4	Document Number Hadley 14"		Rev A00	
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SSID =CHARGER



SSID = PWR.Plane.Regulator_5v3p3v

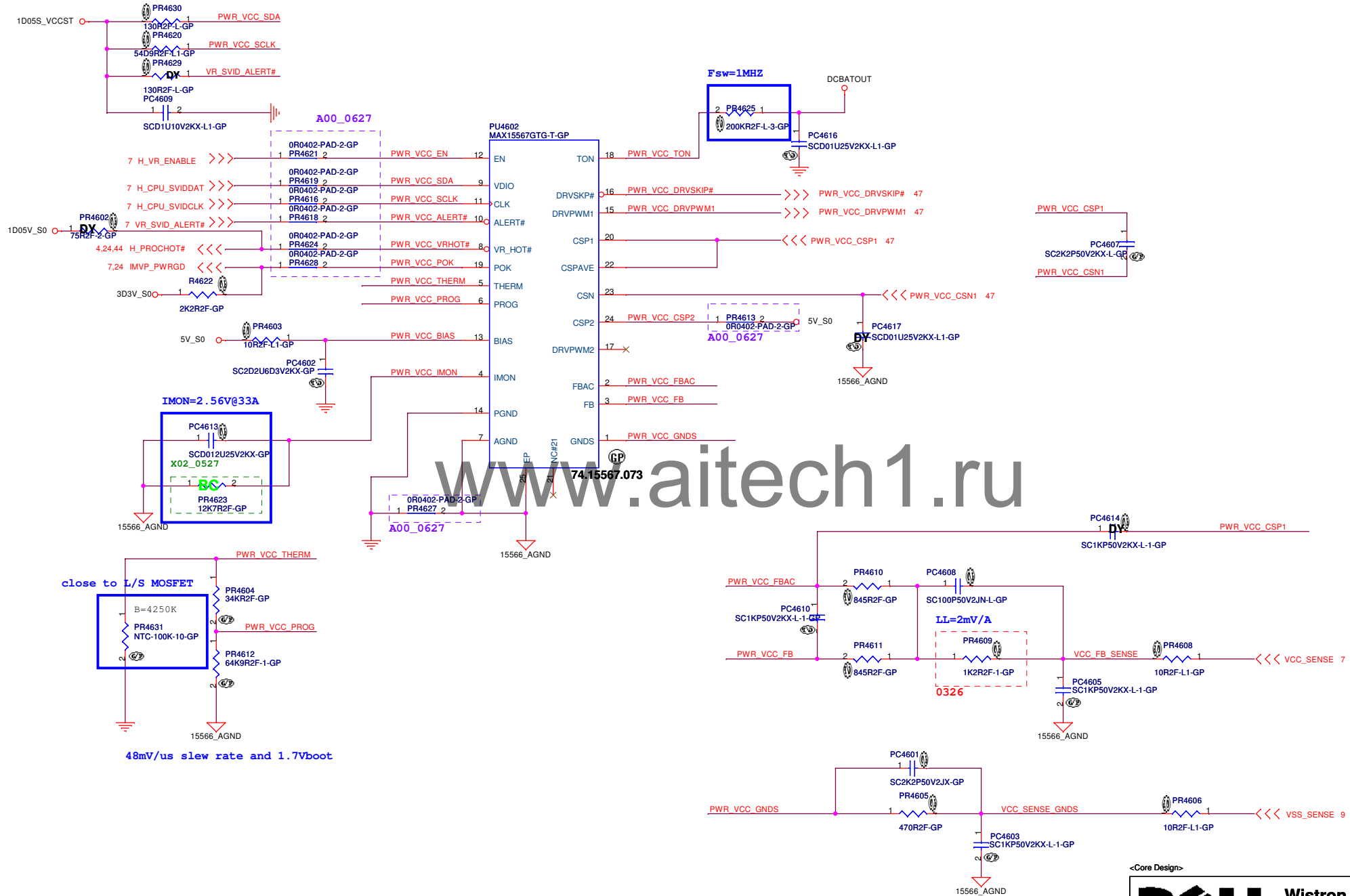


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP T 220U 6.3V M3528 PSL /NEC-TOKIN/ 25mOhm / 77.C2271.45L
H/S,L/S: FET MOS CSD87381P SON 5P/ 15.3m ohm@4.5Vgs/ 7 mohm@ 4.5Vgs / 84.87381.03G

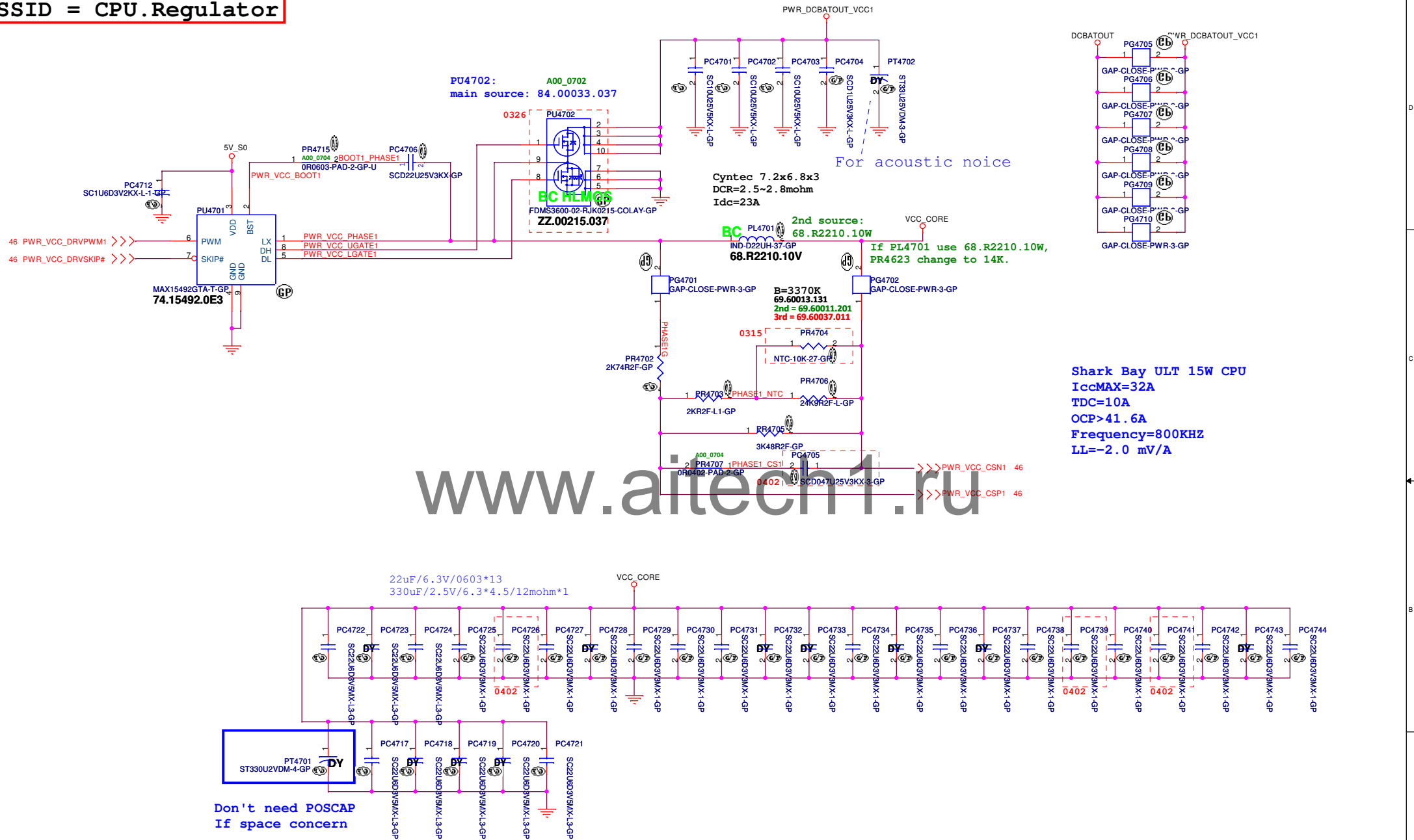
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP T 220U 6.3V M3528 PSL /NEC-TOKIN/ 25mOhm / 77.C2271.45L
H/S,L/S: FET MOS CSD87381P SON 5P/ 15.3m ohm@4.5Vgs/ 7 mohm@ 4.5Vgs / 84.87381.03G

<Core Design>

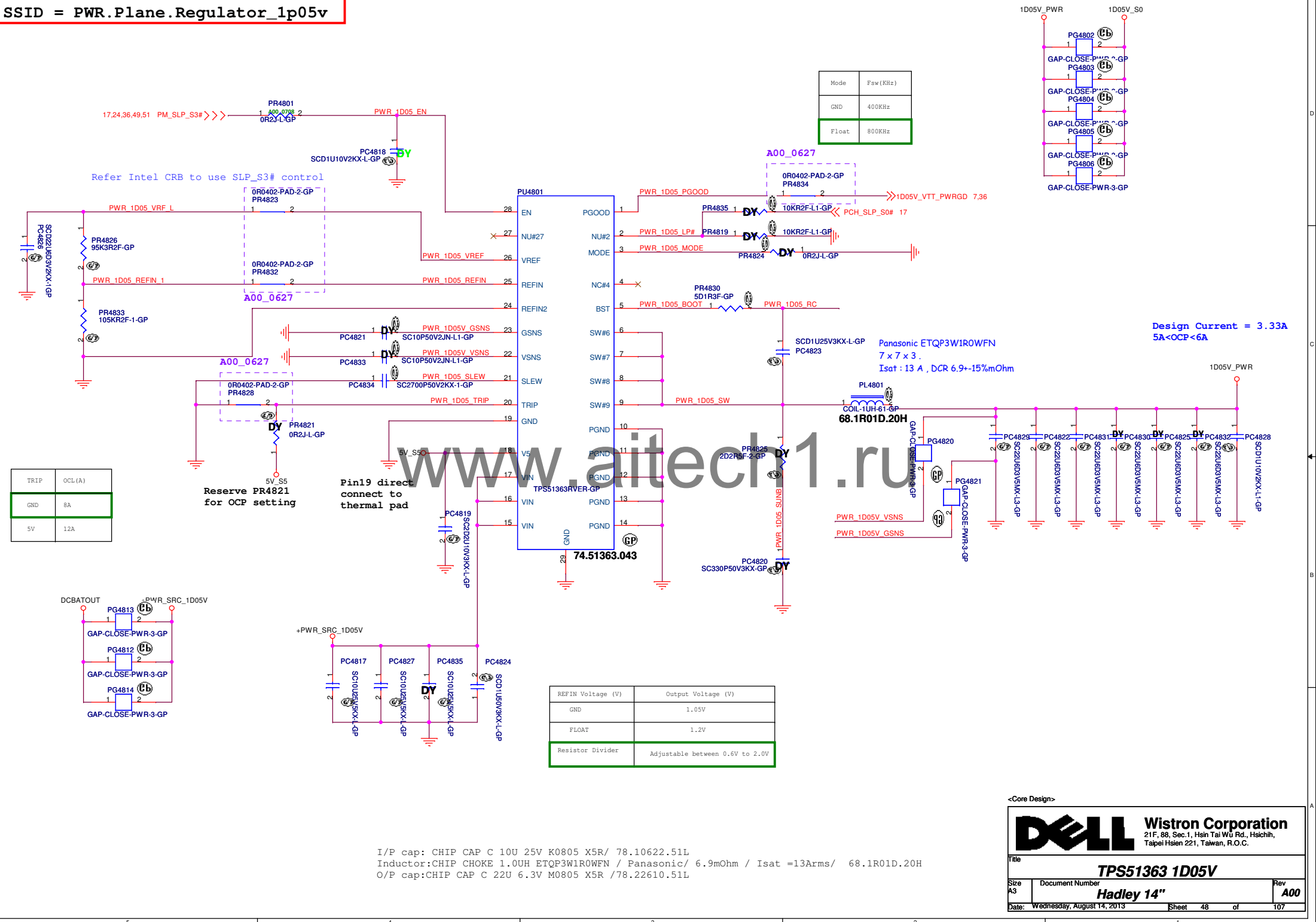
SSID = CPU.Regulator



SSID = CPU.Regulator




SSID = PWR.Plane.Regulator_1p05v



TRIP	OCL (A)
GND	8A
5V	12A

REFIN Voltage (V)	Output Voltage (V)
GND	1.05V
FLOAT	1.2V
Resistor Divider	Adjustable between 0.6V to 2.0V

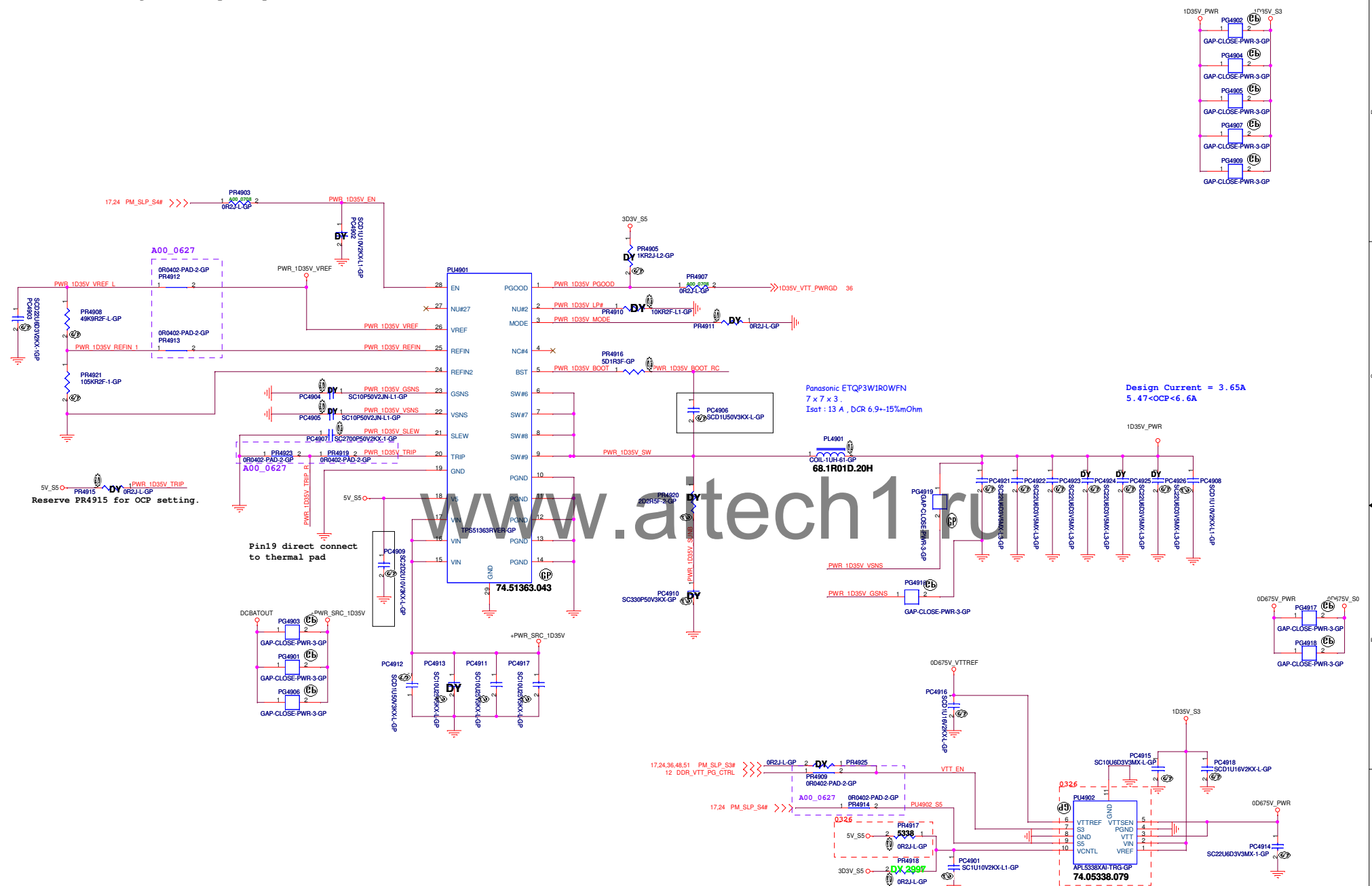
<Core Design>



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Title TPS51363 1D05V		
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I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKR 1.0UH ETQP3WIROWFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L

If use 74.02997.B79, Stuff PR4918 and Dummy PR4917.
2nd source:
74.02997.B79

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Title
TPS51367+51206 1D35V & 0D675V


Size C Document Number
Hadley 14"

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Title

(Reserved)TPS51312 1D8V

Size
A3

Document Number
Hadley 14"

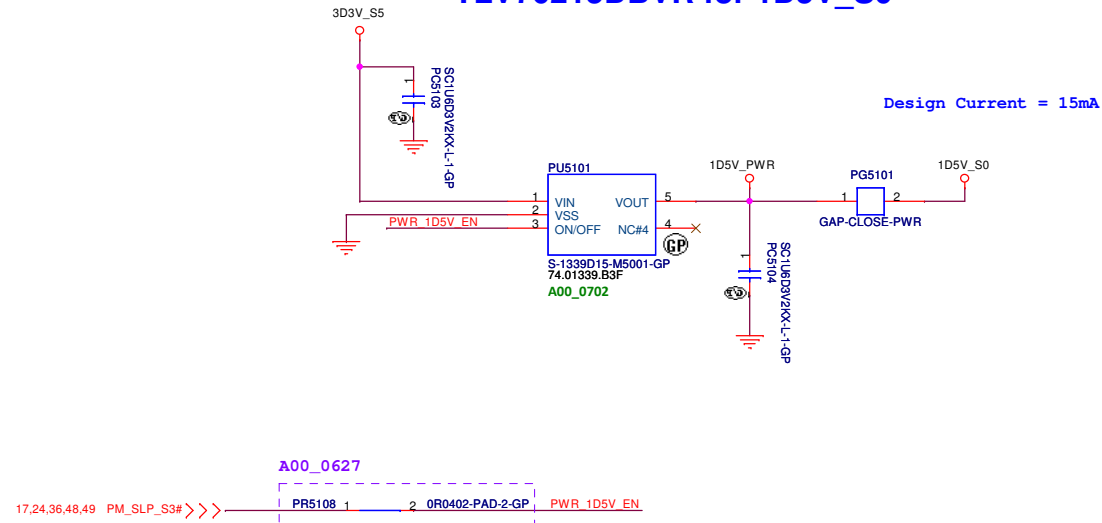
Rev
A00

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SSID = PWR.Plane.Regulator_1p5v

TLV70215DBVR for 1D5V_S0

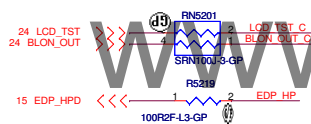
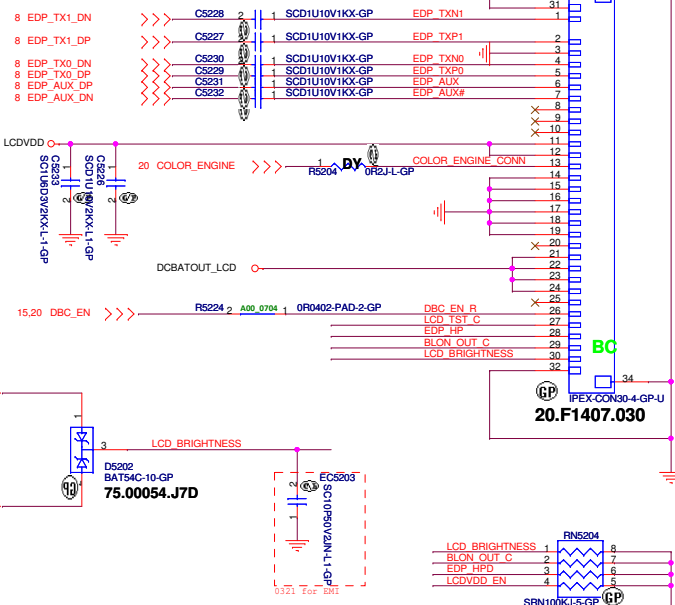
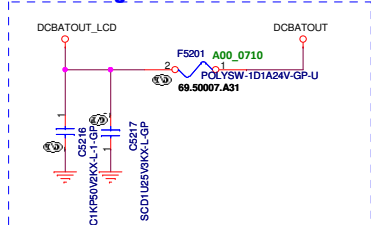


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<Core Design>

LCDVDD

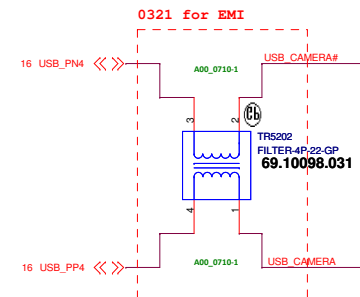
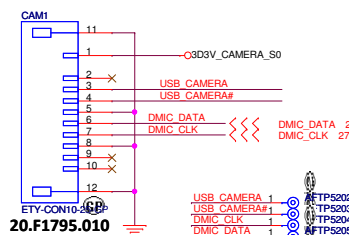
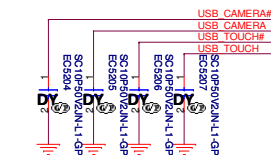
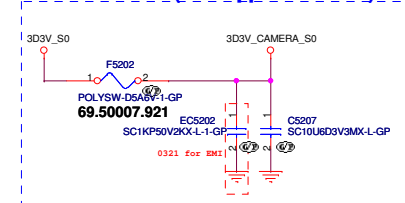
Panel CONN



CAMERA

Camera Power

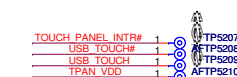
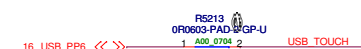
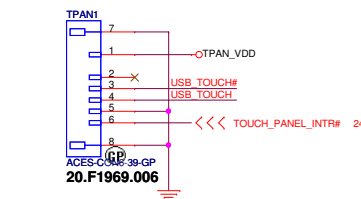
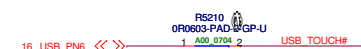
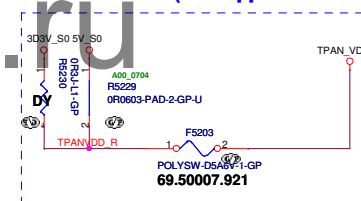
Remove Switch(No support D3 cold)



TPNL

Touch Panel Power

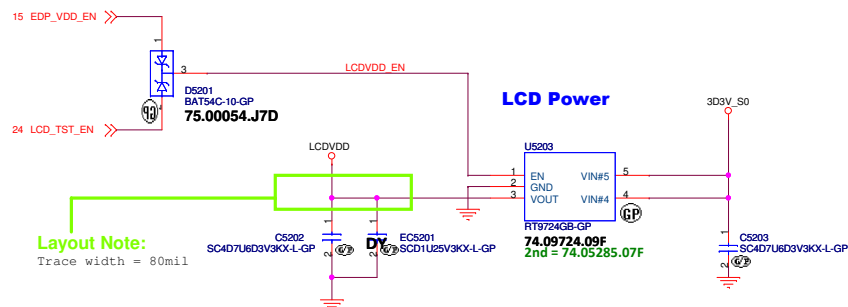
Remove Switch(No support D3 cold)



Layout Note:

Trace width = 80mil

LCD Power



<Core Design>

DELL

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LCD Connector


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Rev	
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Title

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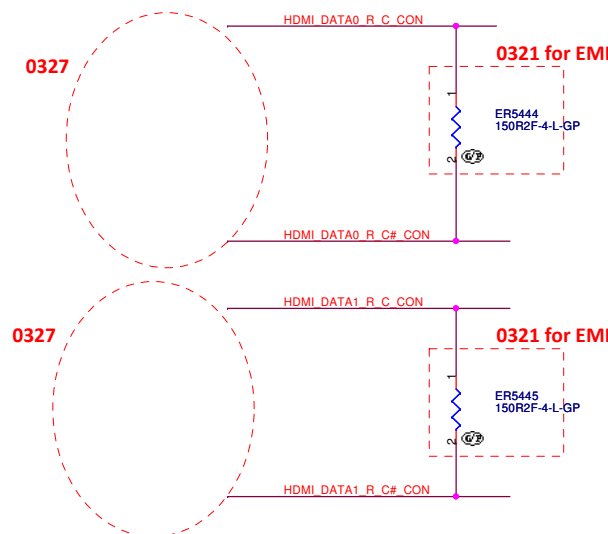
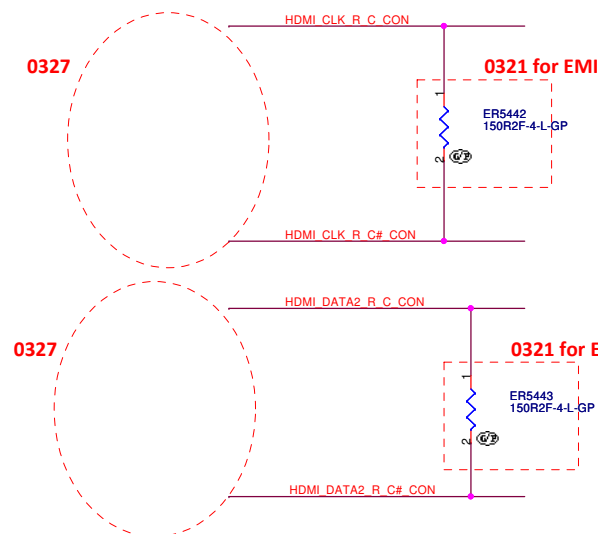
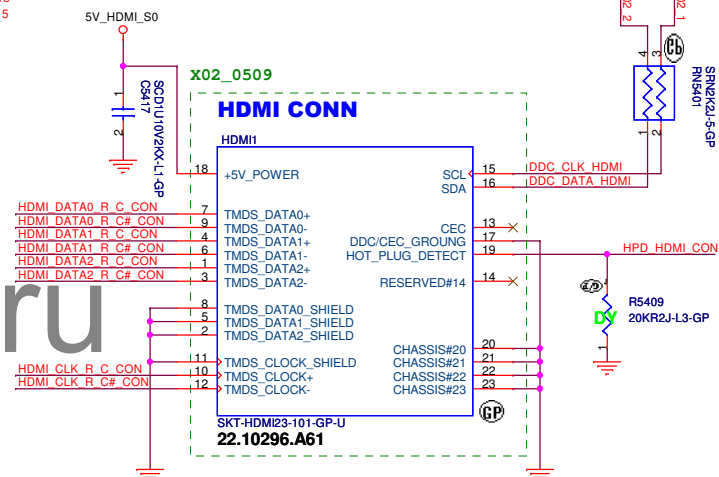
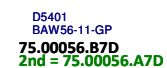
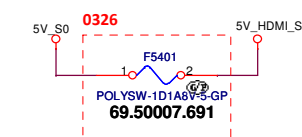
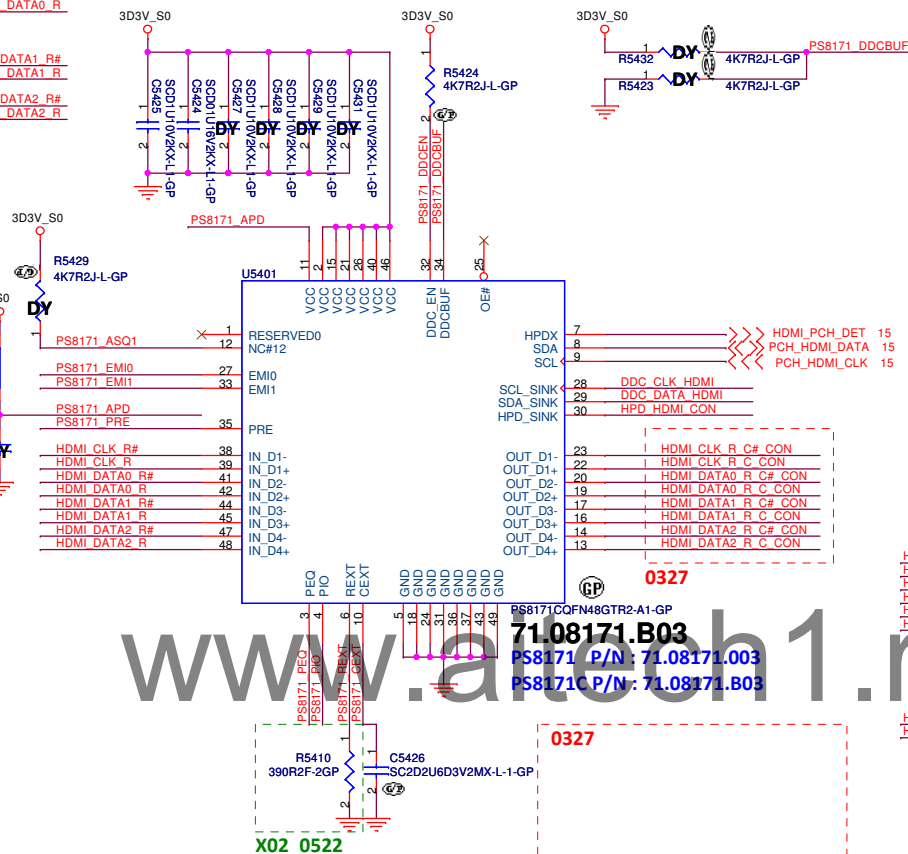
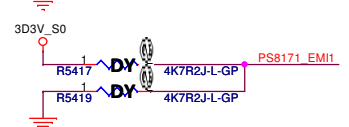
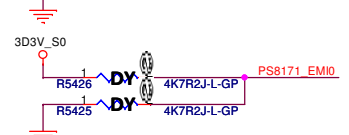
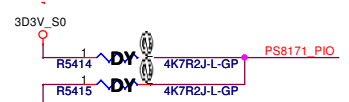
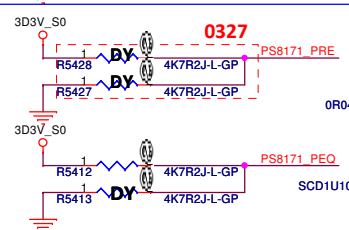
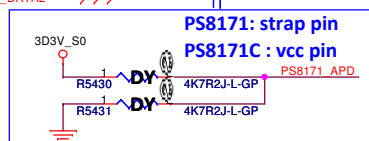
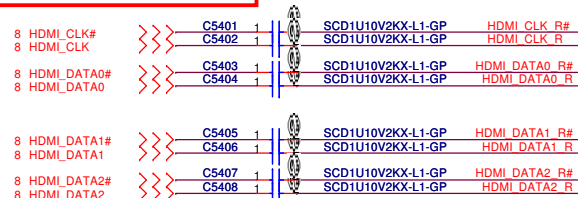
Sheet

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SSID = VIDEO



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SSID = SATA

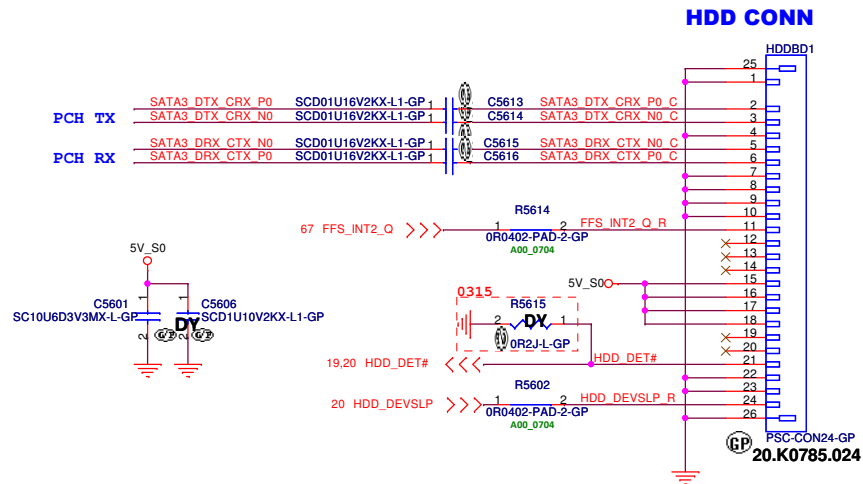
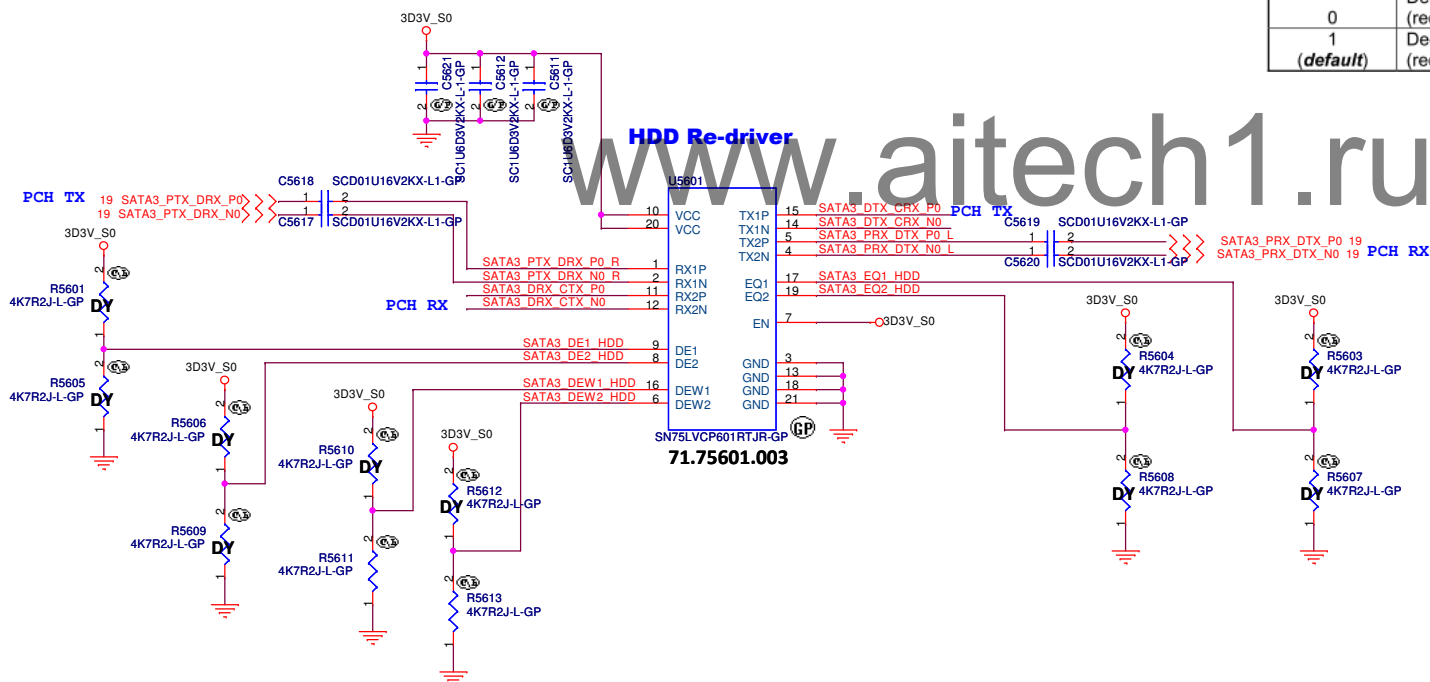


Table 1: Tx/Rx EQ & DE Pulse Width Settings

DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (default)	0
0	7
1	14


DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)



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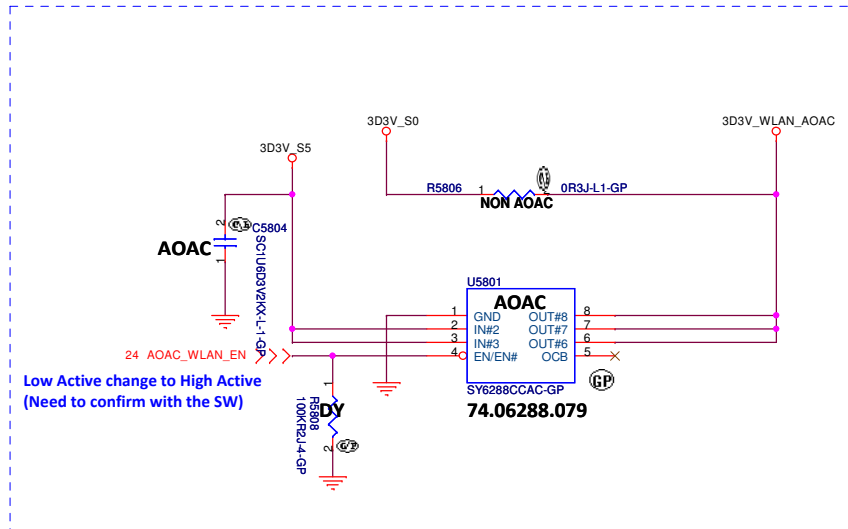
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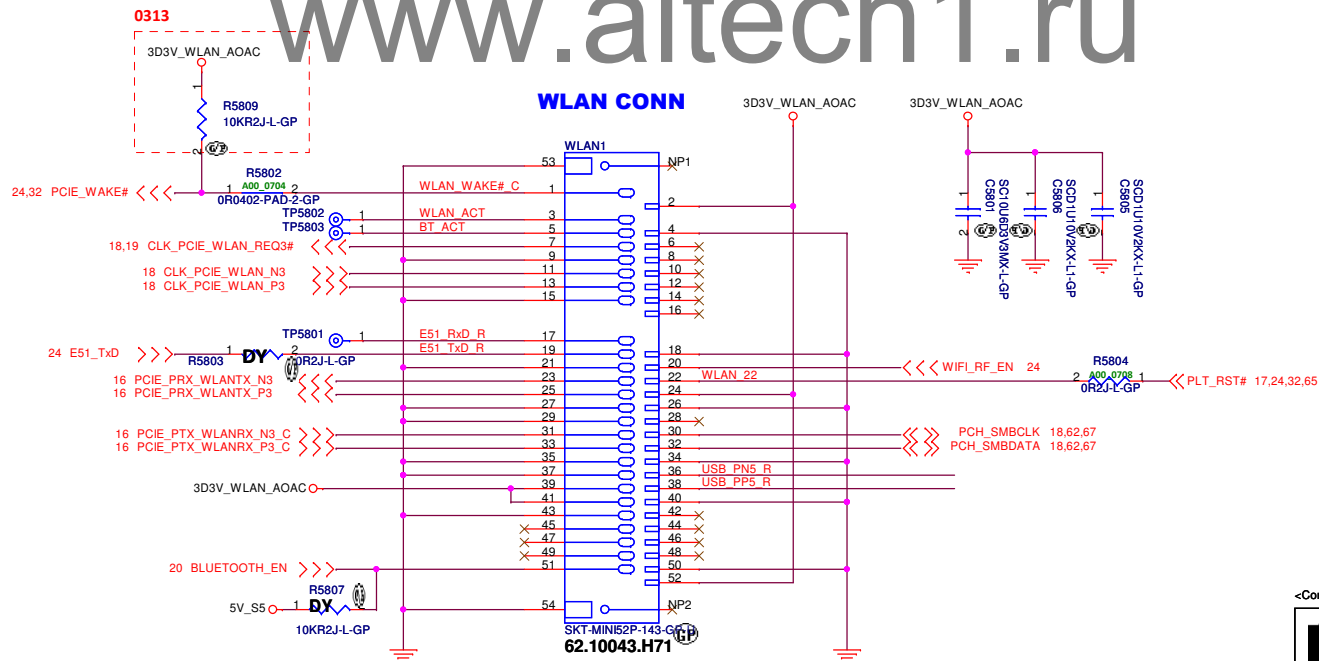
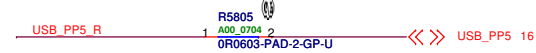
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SSID = Wireless

Change power switch(Active High)



A00_0708



<Core Design>

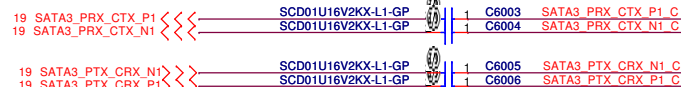
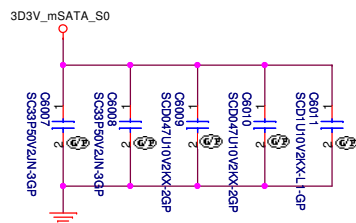
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Title			
WLAN/BT			
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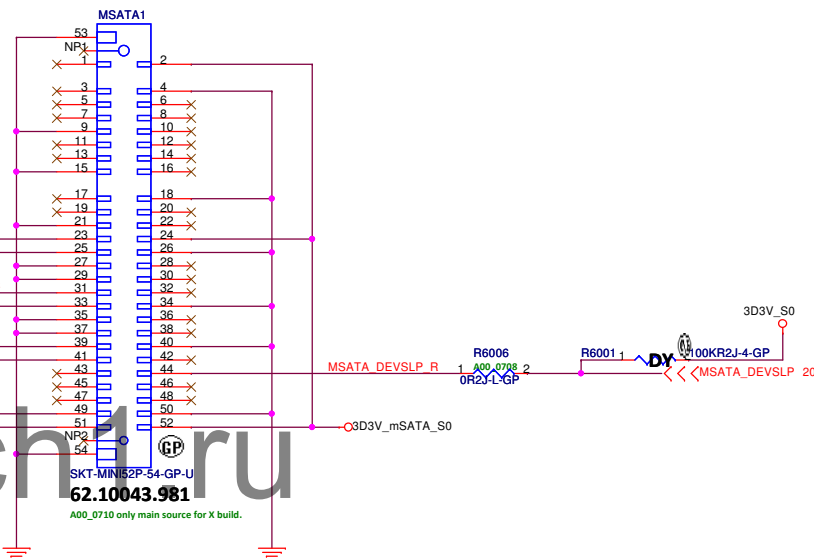
<Core Design>

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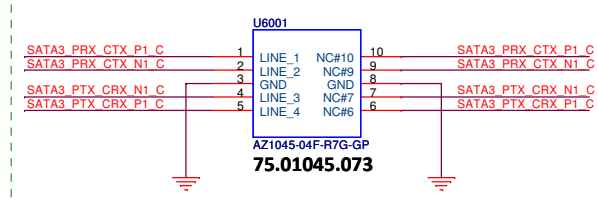
SSID = mSATA



MSATA CONN



X02_0515



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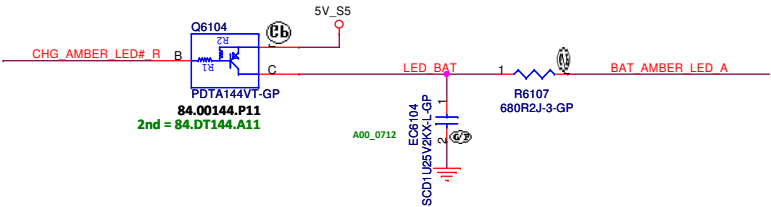
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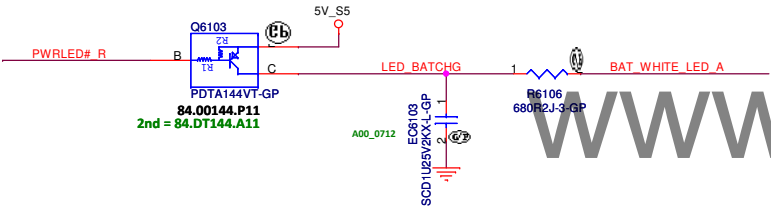
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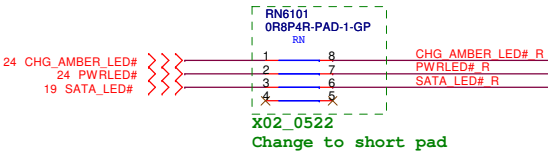
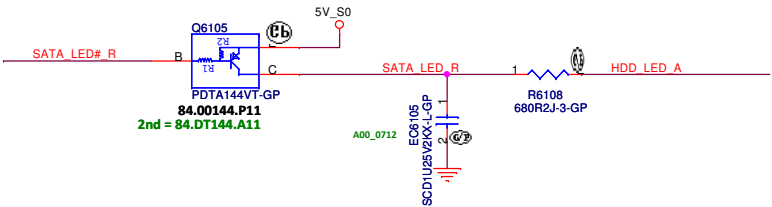
Battery LED1(Amber_LED)
LOW actived from KBC GPIO



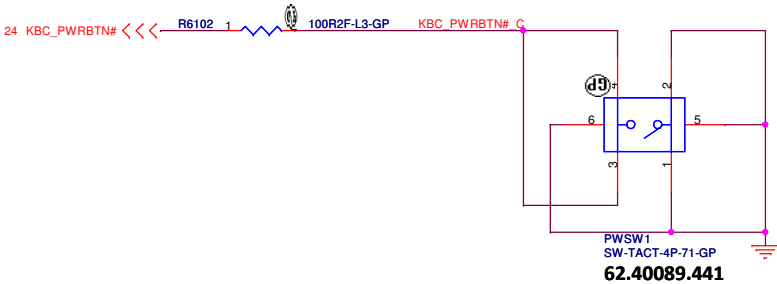
Battery LED2(White_LED)
LOW actived from KBC GPIO



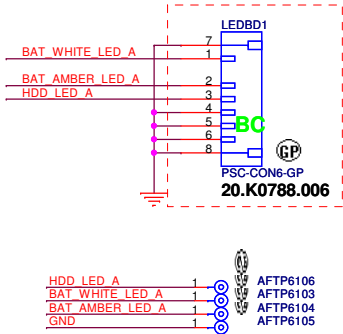
SATA HDD LED
LOW actived from PCH GPIO



PWRBTN



LED board CONN
0313



<Core Design>

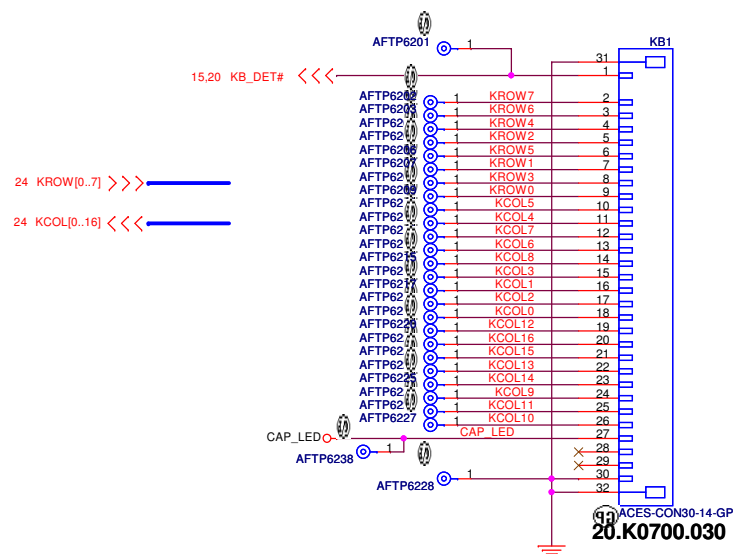


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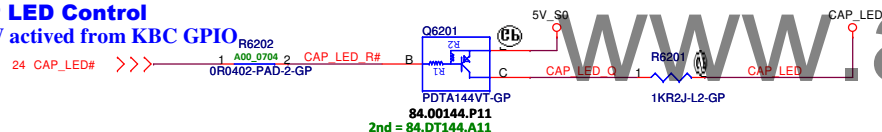
SSID = KBC

Internal Keyboard Connector

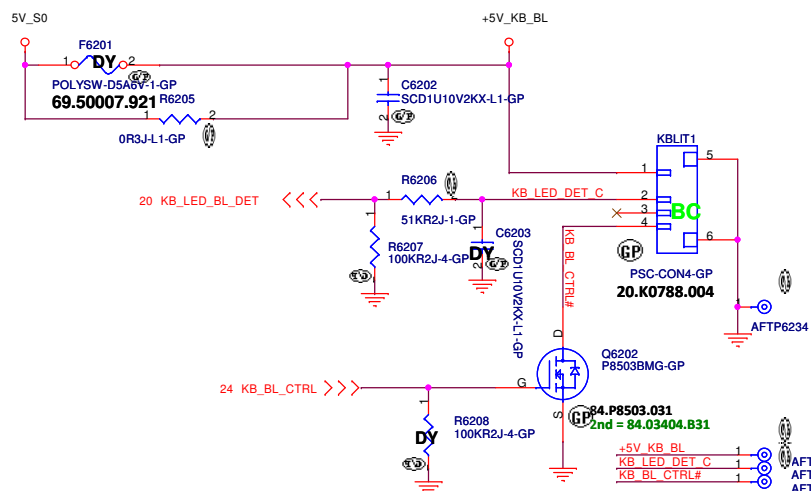


CAP LED Control

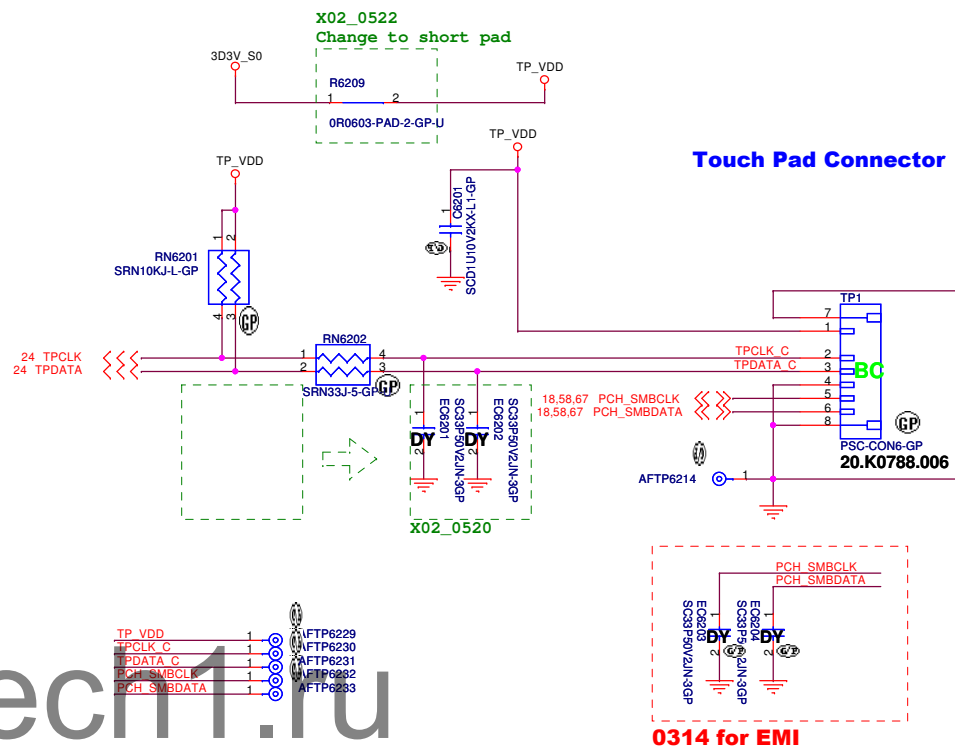
LOW actived from KBC GPIO.



1109 Add KB backlit



```
SSID = Touch.Pad
```



0314 for EMI

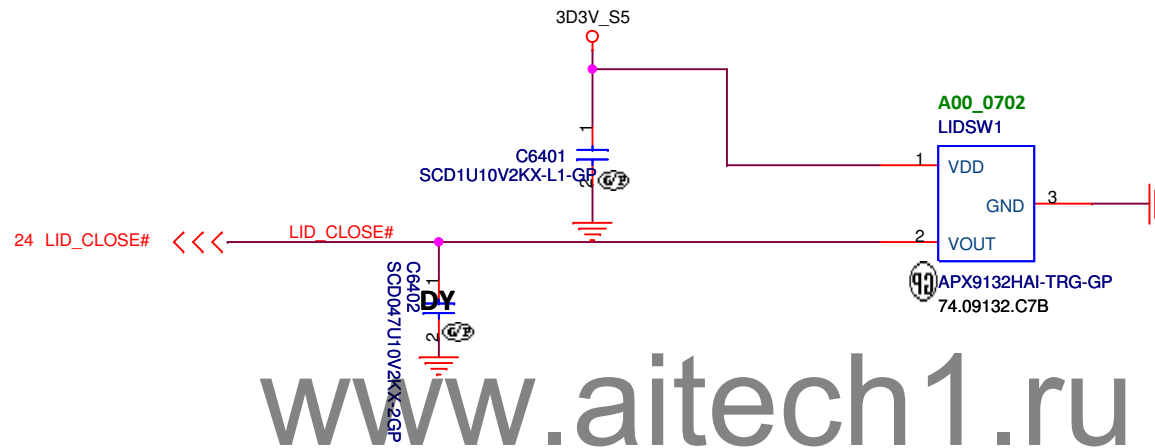
SSID = User.Interface

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SSID = User.Interface



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Title

Hall Sensor

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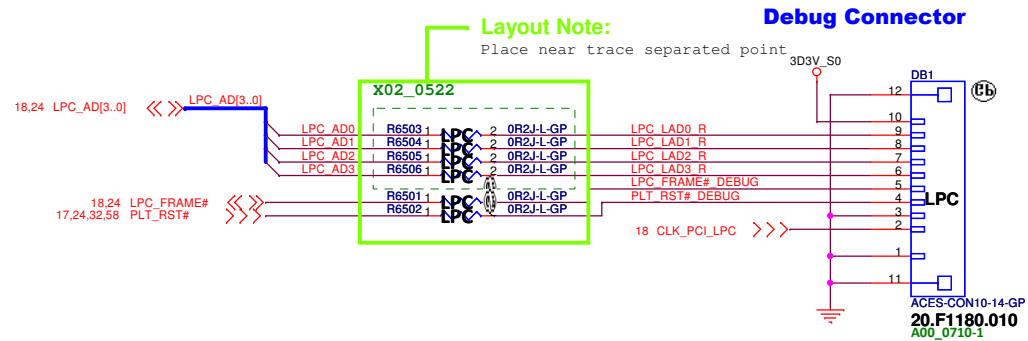
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SSID = DEBUG PORT



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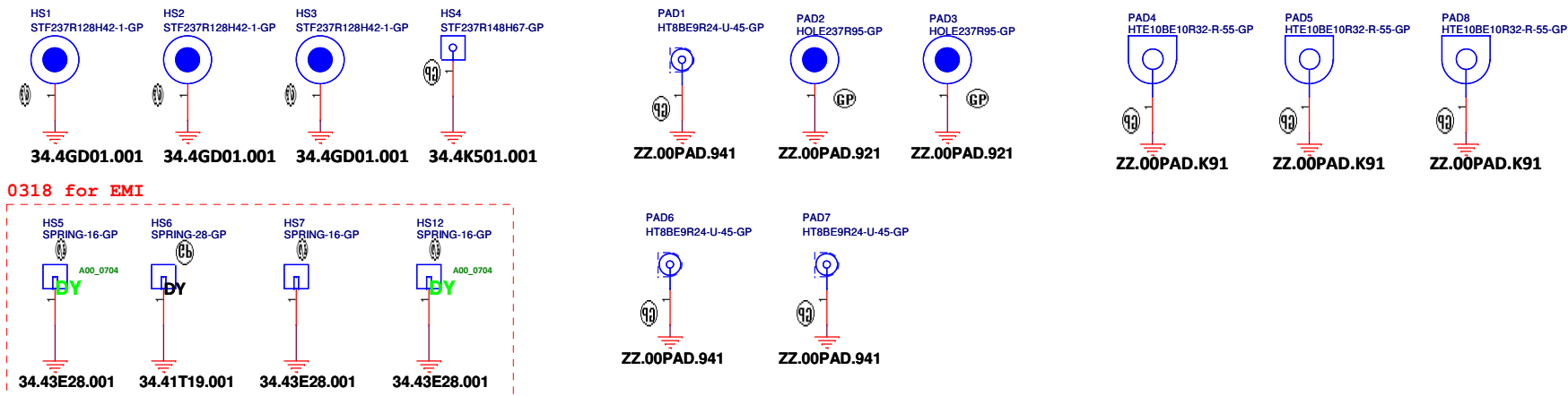
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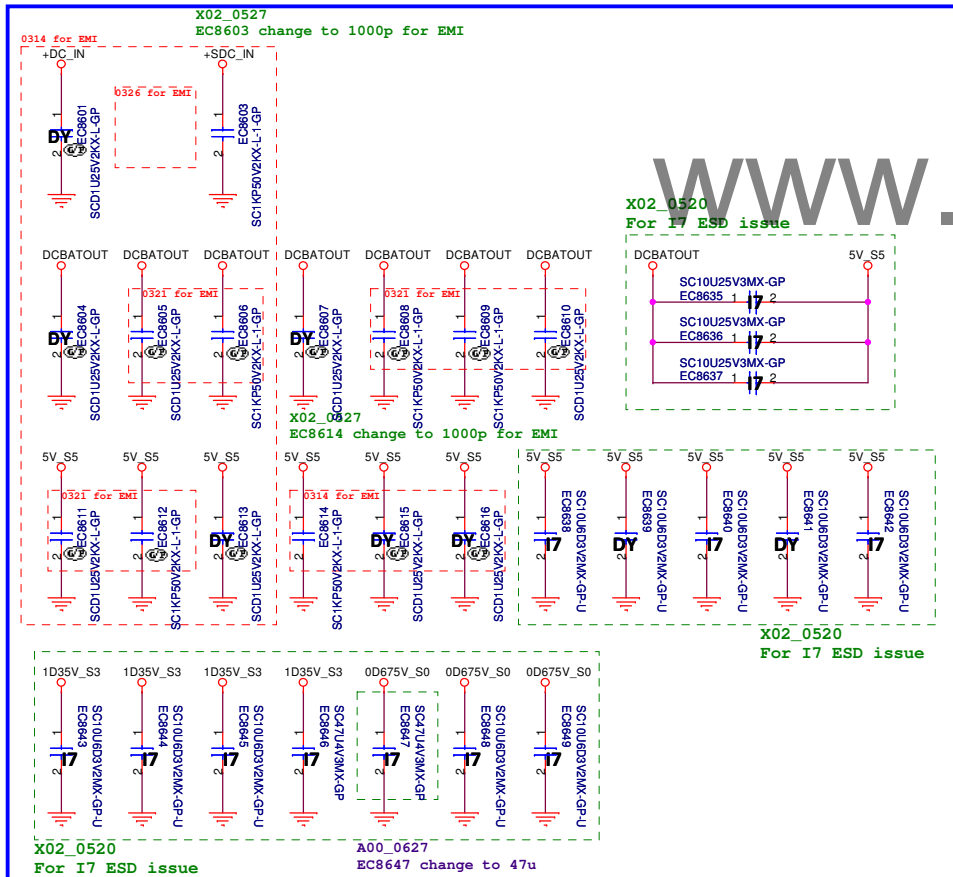
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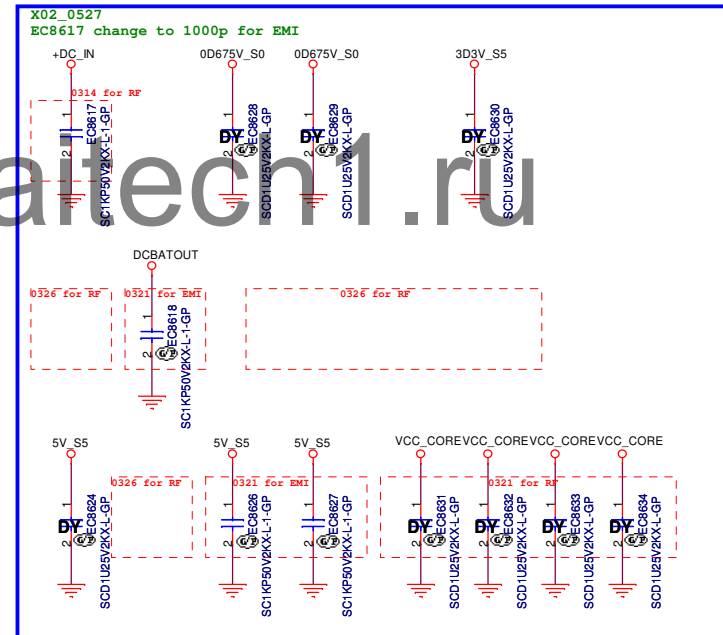
```
SSID = User.Interface
```



For EMI



For RF



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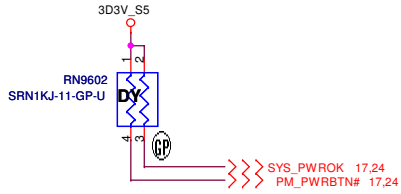
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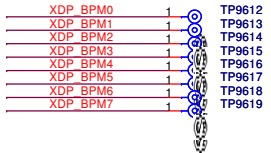
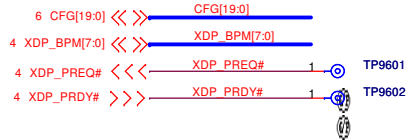
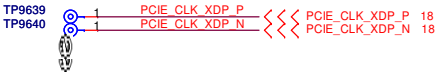
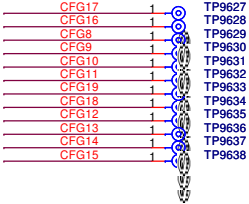
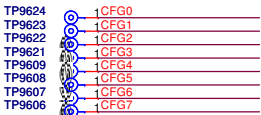
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SSID = XDP



CPU XDP



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PCH Strapping

Name	Schematics	Notes

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
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PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1 (WLAN)
LANE4	X
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	
3	
4	
5	


USB Table

Pair	Device
0	USB port 1, with Power Share
1	USB 2.0 HDMI
2	USB port2 (usb redriver)
3	X
4	Touch Panel
5	Card Reader
6	BLUETOOTH
7	CAMERA

SMBus ADDRESSES

I ² C / SMBus Addresses	CHIEF RIVER ORB	
	Address	Bus
Device EC SMBus 1 Battery 0 CHARGER FS8122 (HDMI Switch) (Bottom Dock) USB3.0 redriver FS8710 (Bottom Dock)	0x16 0x12 0x9E 0x40	BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 Battery 1 PCH Discrete VGA Thermal FS8321 HDMI level shifter NCT7718W	0x16 0x96 & 0x94 0x9C or 0x9E 0x96 & 0x97 0x98 or 0x99	SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
EC SMBus 3 NCT5605Y-0 NCT5605Y-1	0x30 0x32	SMB2_CLK/SMB2_DATA SMB2_CLK/SMB2_DATA SMB2_CLK/SMB2_DATA
PCH SMBus SO-DIMMA SO-DIMMB Intel LAN 82579 G-Sensor MINI WWAN INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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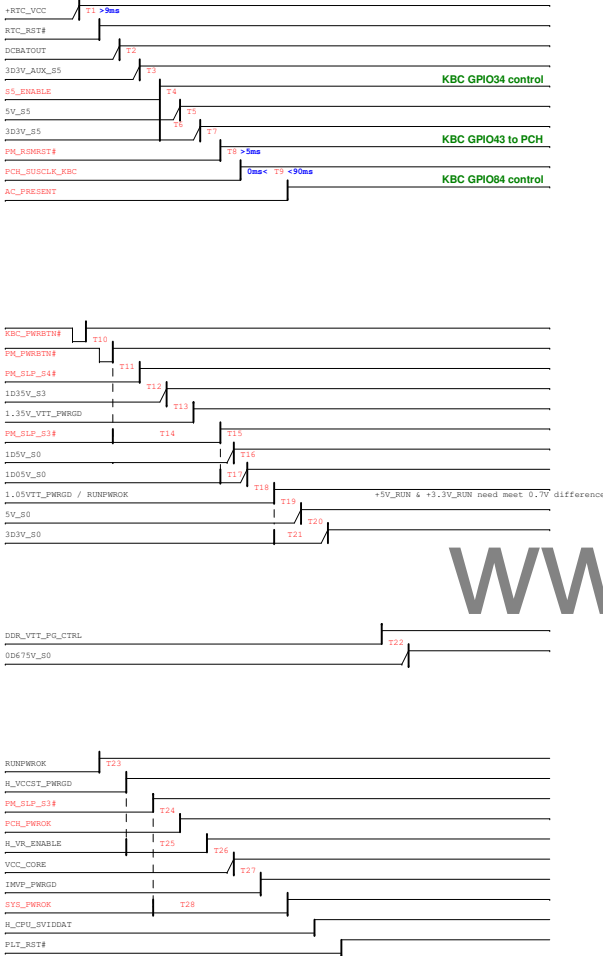
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Intel-Power Up Sequence

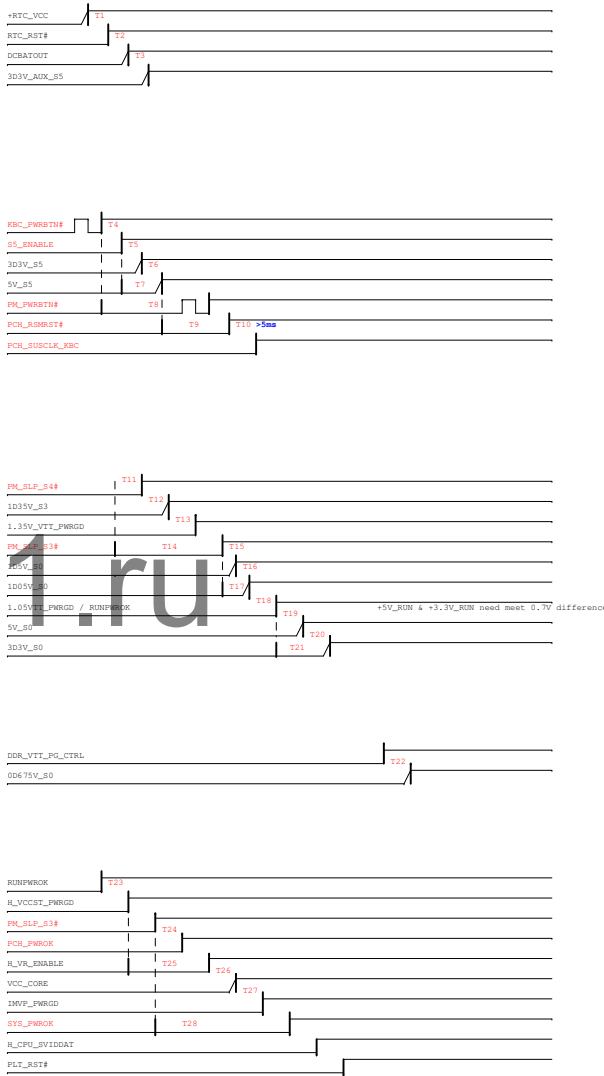
(AC mode)

Red printings:KBC GPIO involved



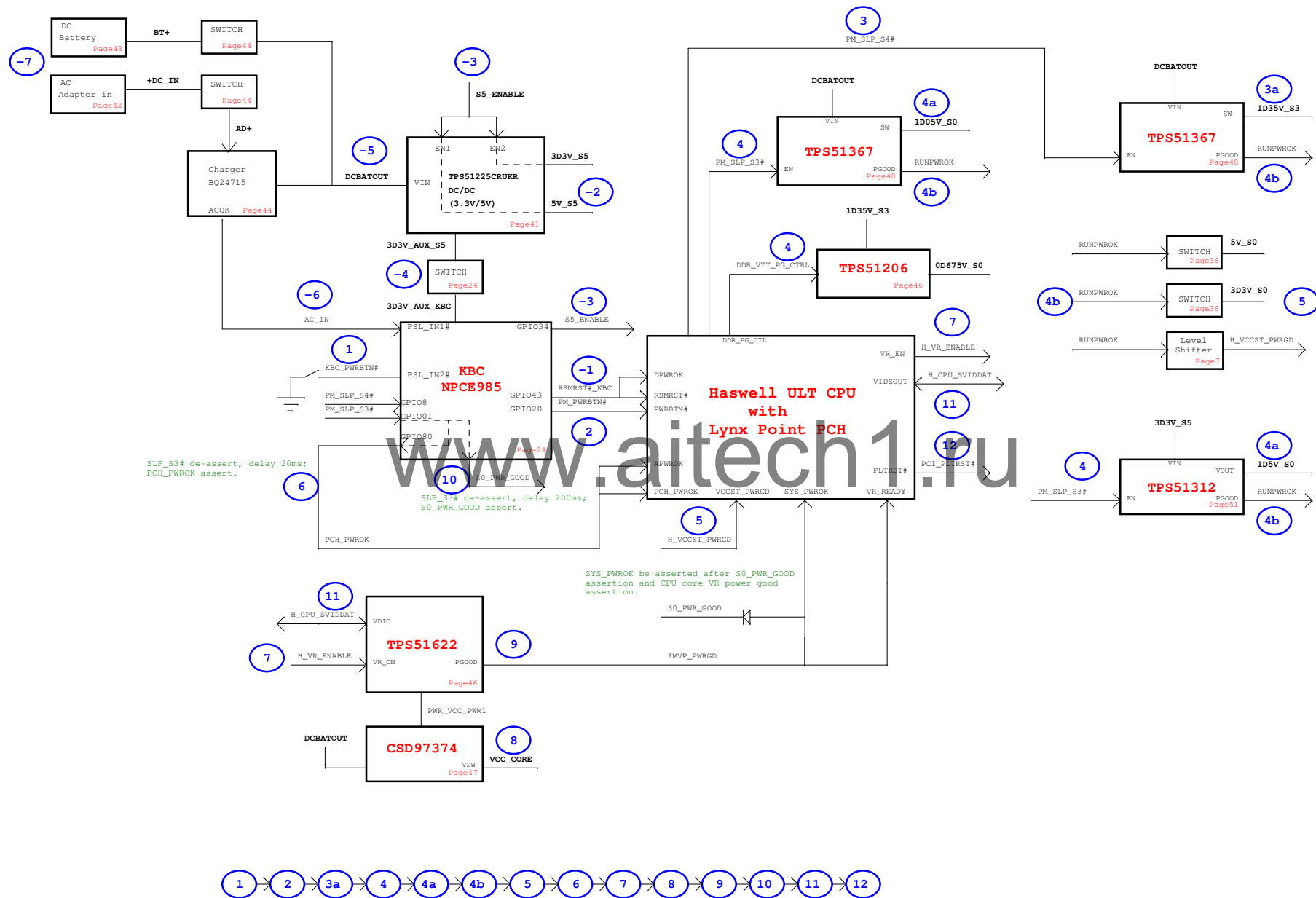
(DC mode)

Red printings:KBC GPIO involved

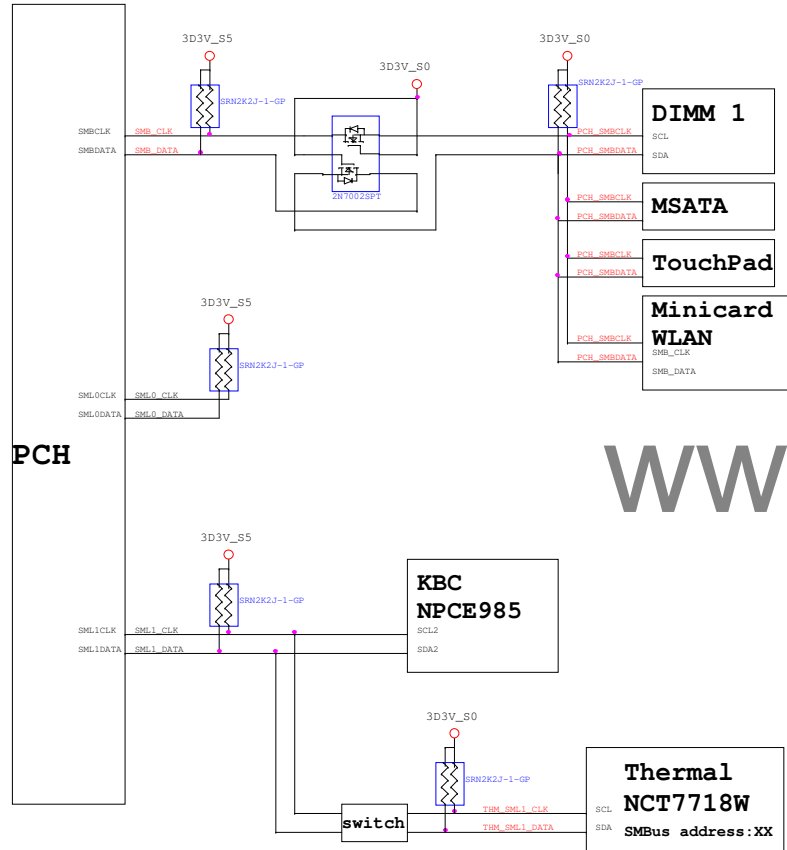


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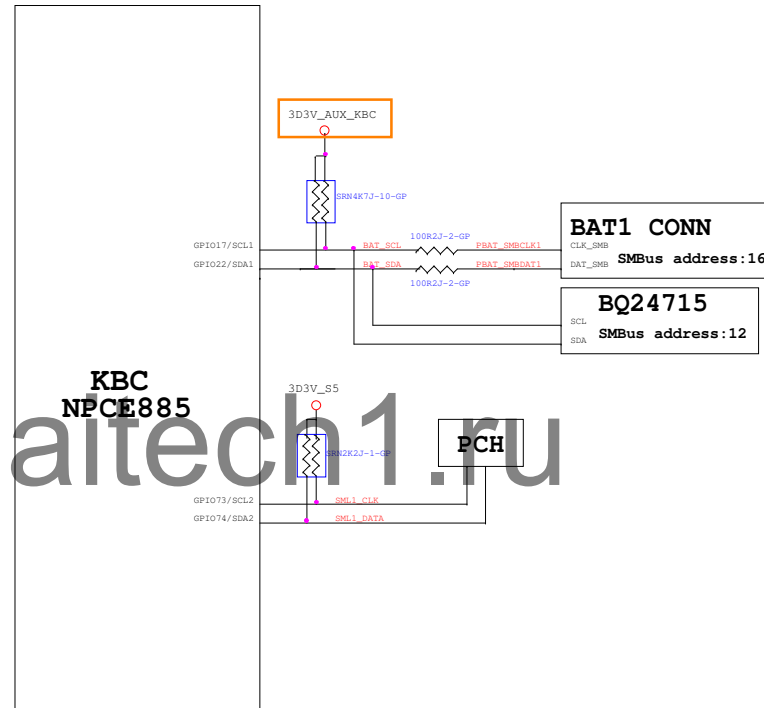
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



PCH SMBus Block Diagram

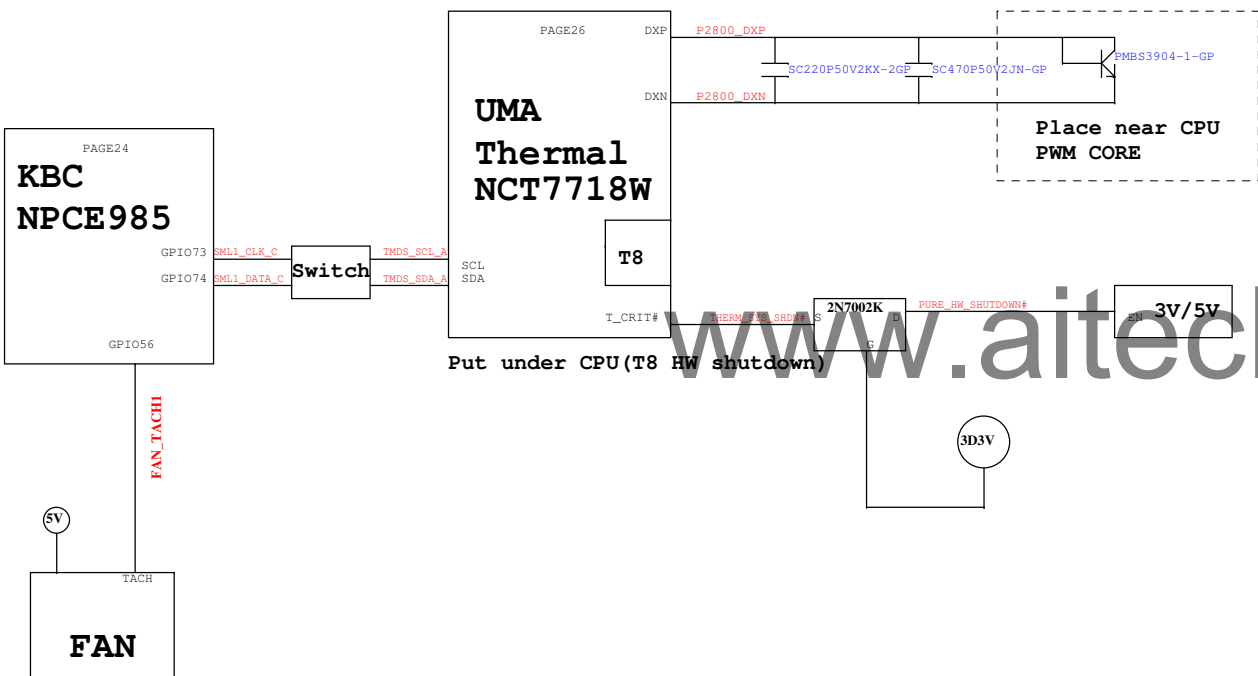


KBC SMBus Block Diagram

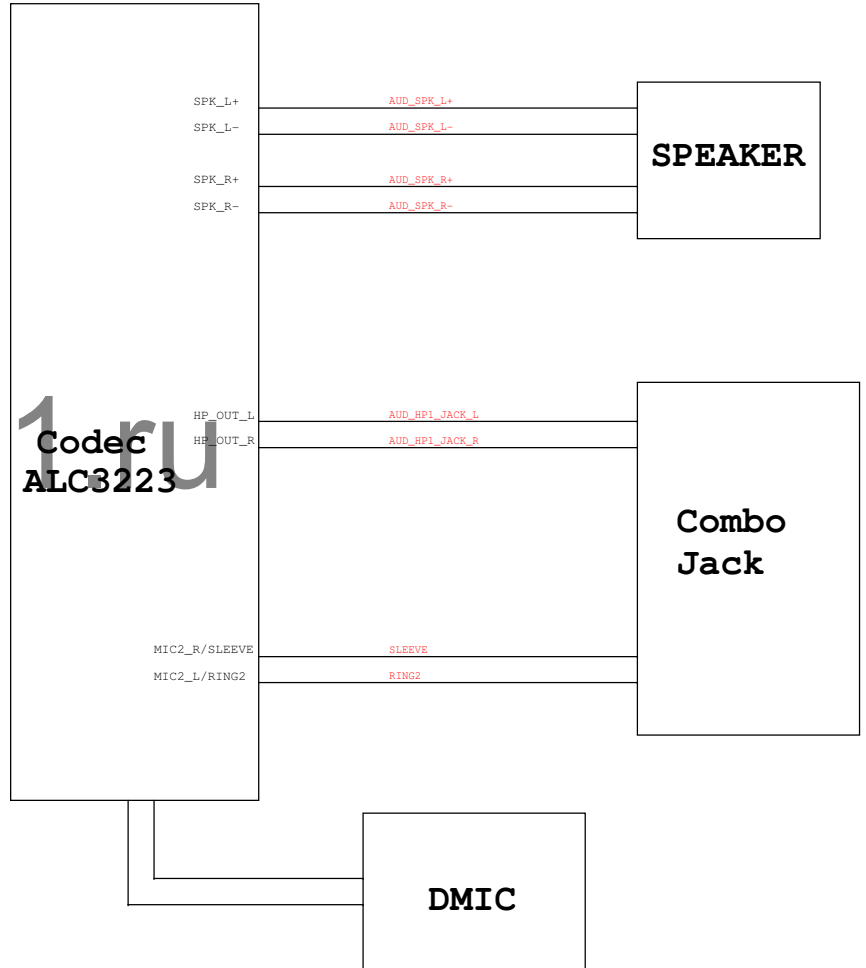


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Thermal Block Diagram



Audio Block Diagram



Item	Pg.	Date	Description	Owner
CPU	7	0313	1.Add C704,C705 D1U cap PD (need close to CPU side)	EE
PCH	20	0313	2.Change R2001,R2007,R2015,R2017,R2019,R2020,R2021,R2023 short pad to 0 ohm.	EE
PCH	15	0313	3.follow DOH50 change R1509 from 10K to 100K	EE
FFS	15,56	0313	4.stuff R1503,R5614 for FFS	EE
KBC	24	0313	5.change R2404 from 10K to 20k for PT config	EE
PCH	18	0313	6.RN1805 8P4R change to 4P2R(RN1808,RN1805) by power well different	EE
SPI	25	0313	7.Remove SKT25 colay	EE
PCH	17	0313	8.change PCH_WAKE# PH R1705 to 1K ohm and change RN1701 to 4P2R 10K	EE
WLAN	58	0313	9.Add R5809 pull high 10k for wifi wake	EE
AUDIO	27,28	0313	10.Delet LINE2_L trace and change to mono_out for tweeter by vendor	EE
LED	61	0313	11.change LEDBD1 P/N to 20.K0788.006 for 6 pin by ME	ME
	17,62,86	0314	12.Add CAP EC6204, EC6203, EC1702, EC8619, EC8620, EC8621, EC8622, EC8623, EC8604, EC8605, EC8606, EC8609, EC8610, EC8617, EC8601, EC8602, EC8603, EC8614, EC8616, EC8615, EC8613, EC8612, EC8611, EC8627, EC8626, EC8625 for EMI	EMI
	18,26	0315	13.SWAP RN2603 and RN1808 net by layout	Layout
LCD	52	0315	14.change TOUCH_PANEL_INTR# to input direction	EE
LCD	24	0315	15.change R2445 to D2402 and dummy for TOUCH_PANEL_INTR#	EE
USB	34	0315	16.DUMMY C3419,C3413,C3411 and change C3414 to 1u by layout location	EE
KBC	24	0315	17.Reserve R2445 for PSL_IN2# Issue	EE
HDMI	54	0315	18.follow DOH50 to change D5401 P/N	EE
	29,44,47	0315	19.change PR4704,U2901,PQ4408 P/N for BOM merge	EE
HDD	19,20,56	0315	20.Reserve R5615 to GND and change MCP_GPIO35 to HDD_DET# for sku option	EE
LCD	24	0315	21.Dummy R2443 for panel site have pull high by vendor	EE

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Item	Pg.	Date	Description	Owner
PCH	18	0318	1.change CLK_PCIE_REQ port by intel EDS	EE
	86	0318	2.HS5, HS6, HS7, HS12 add EMI spring	EMI
Charger	44	0318	3.Dummy PR4459 and stuff PR4458 for 15V_S5 schematic	POWER
Charger	44	0318	4.Dummy PR4441, PR4440, PR4442, PR4447 for DOH40 BATT not unplug	POWER
Charger	44	0318	5.Dummy PQ4412, PR4452, PR4454, PC4409 and PC4431 for DOH40 BATT not unplug	POWER
Charger	44	0318	6.Combin Charger cell pin schematic in PQ4412 and combin AC_IN# and H_PROCHOT# schematic in PQ4413	POWER
Charger	44	0318	7.Add PC4414 by power	POWER
Charger	44	0318	8.PR4436 change to 220K by power	POWER
3V/5V	45	0318	9.Dummy PC4525, PC4526, PC4532, PC4533, PC4534, PC4527, PD4502 and PD4503 for 15V_S5 schematic	POWER
memory	12,13	0318	10.update RAM1~RAM8 P/N and PCBfootprint for memory size	EE
PCH	21	0320	11.Change U2101 part number from 74.22965.093 to 74.59147.093 by meet intel SPEC; remove C2140	EE
USB	35	0320	12.Change USB charger solution and add USB_SW	EE
CPU	7	0320	13.Add TP for N61,N59 by MOW update	EE
AUDIO	28	0320	14.Change tweeter speaker AMP solution for POP noise	EE
PCH	18	0322	15.Change PCIE CLK and REQ# Port mapping	EE
HDMI	54	0322	16.Stuff R5427,R5428 and change R5410 to 487ohm for HDMI fine tune	EE
AUDIO	28	0322	17.Change U2801 to TPA2011D1 for POP noise Change R2805 to 3D3v_S0 and DY Change R2808/R2806 to 165Kohm by vendor Change C2805/C2807 to 0.1u by vendor Add R2813,R2814,R2815,R2816,C2808,U2802,U2803,Q2801 for depop	EE
	52,86	0322	18.Add EC8631~EC8634 0.1u on VCC_CARE and change EC5208~EC5213 to 0402 SIZE for RF	RF
	34,52	0322	19.Stuff TR3403,TR3407,TR5202 CMC,U3401,U3402 TVS and DY R3409,R3411,R3403,R3403,R5214 ,R5217 for EMI	EMI

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Item	Pg.	Date	Description	Owner
	54	0322	1.Change R5442,R5443,R5444,R5445 to ER5442,ER5443,ER5444,ER5445 150ohm and stuff for EMI	EMI
	54	0322	2.Remove TR5402,TR5403,TR5404,TR5405 for EMI	EMI
	27	0322	3.Change R2714,R2716,C2723,C2724 to ER2714,ER2716 33ohm ,EC2723,EC2724 22p and stuff for EMI	EMI
	29	0322	4.Stuff EC2901, EC2902, EC2903, EC2904, EC2910, EC2911 1000p for EMI	EMI
	44	0322	5.Add EC4401 1000p on +VCHGR for EMI	EMI
	43	0322	6.Stuff EC4304 1000p on BT+ for EMI	EMI
	86	0322	7.Stuff EC8609,EC8606,EC8618,EC8608 1000p on DCBATOUT for EMI	EMI
	86	0322	8.Stuff EC8610,EC8605 0.1u on DCBATOUT for EMI	EMI
	27	0322	9.Add EC2710~EC2714 0.1u AGND to GND for EMI	EMI
	52	0322	10.Stuff EC5203 10p on LCD_BRIGHTNESS for EMI	EMI
	18	0322	11.Stuff EC1803 22p on SPI_CLK for EMI	EMI
	18	0322	12.Stuff EC1801 22p and R1805 33 ohm on CLK_PCI_KBC for EMI	EMI
	4	0322	13.Reserve EC401 1000p on XDP_TRST# for EMI	EMI
	4	0322	14.Reserve EC402 1000p on H_CPUPWRGD for EMI	EMI
	7	0322	15.Reserve EC701 1000p on H_VCCST_PWRGD for EMI	EMI
	86	0322	16.Stuff EC8626,EC8627,EC8612 1000p on 5V_S5 for EMI	EMI
	86	0322	17.Stuff EC8611 0.1u on 5V_S5 for EMI	EMI
	52	0322	18.Stuff EC5202 1000p on 3D3V_CAMERA_S0 for EMI	EMI
	44,54	0326	19.change F5401,PD4402 symbol by net file check	EE
	86	0326	20.Remove EC8625, EC8623, EC8622, EC8621, EC8620, EC8619 by RF	RF
	86	0326	21.Audio codec: ER2716 change to 100 ohm; ER2714 change to 0 ohm; EC2723, EC2724 dummy EC2905, EC2906, EC2907, EC2908 change to 100pF	EMI

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	33	0326	1.Card reader: EC3302, EC3303, EC3305,EC3306, EC3307 change to 4.7pF	EMI
Charger	44	0326	2.Charger:Dummy PR4401, PR4420 and PQ4411 for DOH40 only 45W adapter Change PR4428 change to 113K by power Dummy PR4449 by power PG4407, PG4403, PG4404 and PG4405 change to ZZ.CLOSE.001 by power PU4405 chnage main source to 84.06675.030	POWER
VCORE	46,47	0326	3.Vcore:PR4609 change to 1.2K and PR4623 change to 11.8K by power PU4702 main source change to 84.03664.037 by power	POWER
0.675V	49	0326	4.0.675V:PU4902 change main source to 74.05338.079 by power Stuff PR4917 and Dummy PR4918 by power	POWER
DCIN	42	0326	5.DCIN:PU4201 chnage main source to 84.06675.030	POWER
PCH	18	0327	6.Change C1801 and C1802 to 15P by vendor	EE
HDMI	54	0327	7.HDMI:Remove R5434~R5441 0402 0 ohm and R5401~R5408 0603 0 ohm by HDMI vendor DY R5427,R5428 by EA test	EE
	86	0327	8.Delet EC8602 by EMI	EMI
CPU	18	0329	9.Change RN1803,RN1804 to R1813~R1816 10K ohm by Intel EDS	EE
CPU	19	0329	10.Change C1903 and C1904 to 15P by vendor	EE
VCORE	45	0402	11.Stuff PC4741, PC4726 and PC4739 and change PC4705 to 78.47322.2BL by power	POWER
Charger	44	0410	12.Change PL4401 to 68.2R21C.10Q by HALT test	EE
CPU	21	0509	13.Add C2148 0.47uF for VccDSW3_3 and DcpSusByp to address temporary inrush currents.	EE
HDMI	54	0509	14.Change HDMI1 to 22.10296.A61 by ME	EE
MSATA	60	0514	15.Reserved U6001 for EMI test	EMI
MSATA	60	0515	16.Change U6001 P/N to 75.01045.073 by EMI	EMI
KBC	24	0515	17.DUMMY RSTSW1	EE
AUDIO	28,29	0515	18.DUMMY Twitter function and remove EC2910, EC2911	EE
AUDIO	29	0515	19.Change SPK1 P/N to 20.F2060.004	ME

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KBC	24	0515	1.Change R2404 from 20K to 33k for ST config	EE
CPU	17,19	0520	2.Add D1901~D1904, EC1703~EC1708 for EMI	EMI
	24,45	0520	3.Add EC2423, EC2424, EC4501 for EMI	EMI
CPU	4,18	0520	4.Add ER411, EC403, EC1804 for EMI	EMI
TPAD	62	0520	5.Shift EC6201 and EC6202 to TPCLK_C and TpDATA_C for EMI	EMI
	86	0520	6.Add EC8635~EC8649 for EMI	EMI
CPU	17,19	0522	7.Remove D1901~D1904 and reserved EC1901~EC1904	EMI
	32	0522	8.CARD32 Change to RTS5227E	EE
HDMI	54	0522	9.Change R5410 to 390ohm	EE
		0522	10.Change R404, R711, R1101, R1102, R1103, R1104, R1105 R1238, R1501, R1807 , RN1806, R1904, R2101, R2103, R2105, R2108, R2112, R2117, R2118, R2401, R2402, R2408, R2409, R2410, R2417, R2427, R2428, R2430, R2440, RN2601, R2706, R2708, R2711, R2718, R2917, R3402, R3702, R3705, RN6101, R6209 to short pad	EE
	65	0522	11.Remove RN6501 and add R6503~R6506 for EE	EE
	19	0523	12.Remove EC1903, EC1904 and add TP1903, TP1904	EMI
CPU	11	0523	13.Change R1102 and R1103 P/N to ZZ.00PAD.M21	EE
	86	0527	14.Change EC8614, EC8617, EC8603 to 1000p for EMI	EMI
	4	0527	15.EC402, EC401 add 1KP for EMI	EMI
	86	0527	16.EC8635, EC8636, EC8637, EC8638, EC8640, EC8642, EC8643, EC8644, EC8645, EC8648, EC8649 add 10uF for EMI, just for I7 config	EMI
	86	0527	17.EC8646, EC8647 add 47uF for EMI, just for I7 config	EMI
	27	0527	18.Change EC2723, EC2724, EC2701, EC2702 to 5.6pF for RF request	RF
	46	0527	19.PR4623 change to 12.7K for power	EE
	44,45 46,48 49,51	0627	20.Change PR4430, PR4413, PR4406, PR4438, PR4417, PR4457, PR4455, PR4446, PR4520, PR4504, PR4502, PR4505, PR4621, PR4619, PR4616, PR4618, PR4624, PR4628, PR4627, PR4613, PR4801, PR4823, PR4832, PR4828, PR4834, PR4903, PR4912, PR4913, PR4923, PR4907, PR4919, PR4909, PR4914, PR5108 to short pad	EE

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	44	0627	1.Change PD4405 to short pad	EE
	24	0627	2.Change R2404 to 64.9K	EE
	15	0628	3.HDD_FALL_INT connect to PIRQB#	EE
	20	0814	4. Add Micron into memory matrix	EE

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